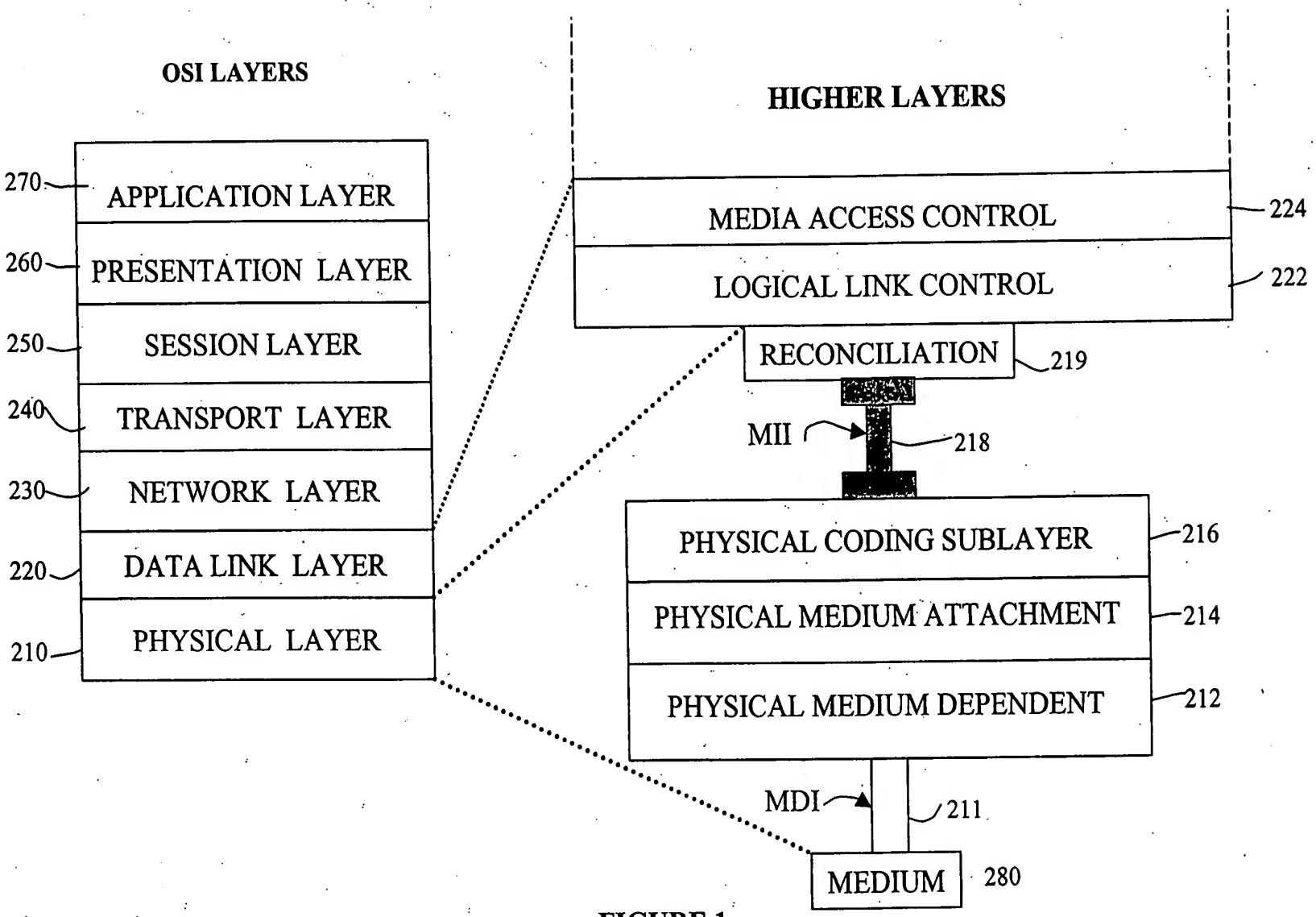

OSI LAYERS
HIGHER LAYERS
270
APPLICATION LAYER
260
PRESENTATION LAYER
250
SESSION LAYER
240
TRANSPORT LAYER
230
NETWORK LAYER
220
DATA LINK LAYER
210
PHYSICAL LAYER
MEDIA ACCESS CONTROL
224
LOGICAL LINK CONTROL
222
RECONCILIATION
219
MII
218
PHYSICAL CODING SUBLAYER
216
PHYSICAL MEDIUM ATTACHMENT
214
PHYSICAL MEDIUM DEPENDENT
212
MDI
211
MEDIUM
280

FIGURE 1

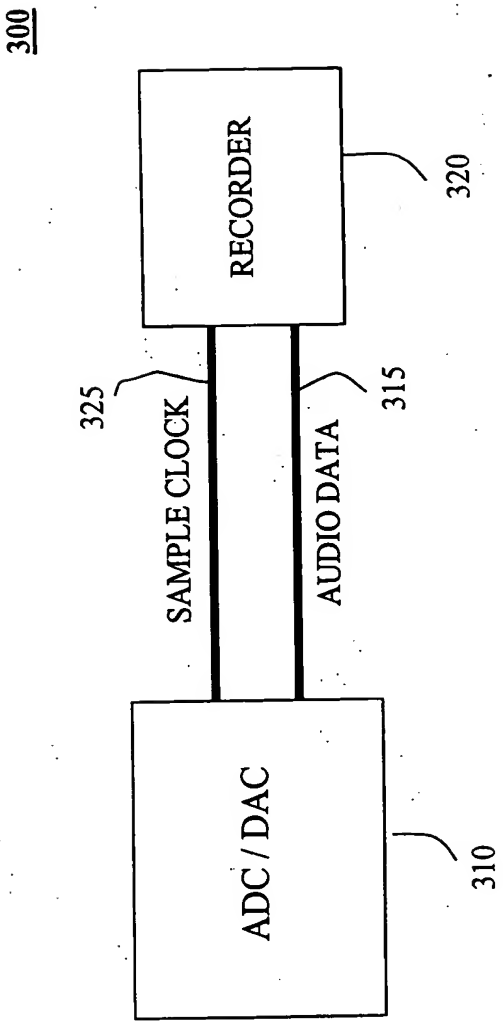


FIGURE 2

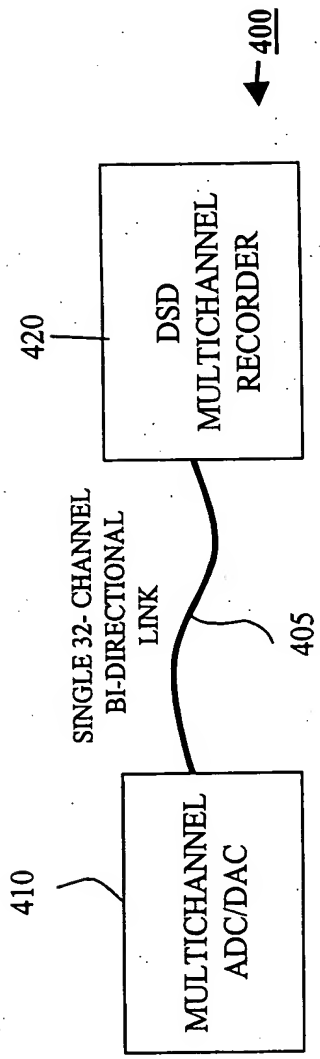

400
420
DSD
MULTICHANNEL
RECORDER
SINGLE 32- CHANNEL
BI-DIRECTIONAL
LINK
405
410
MULTICHANNEL
ADC/DAC

FIGURE 3

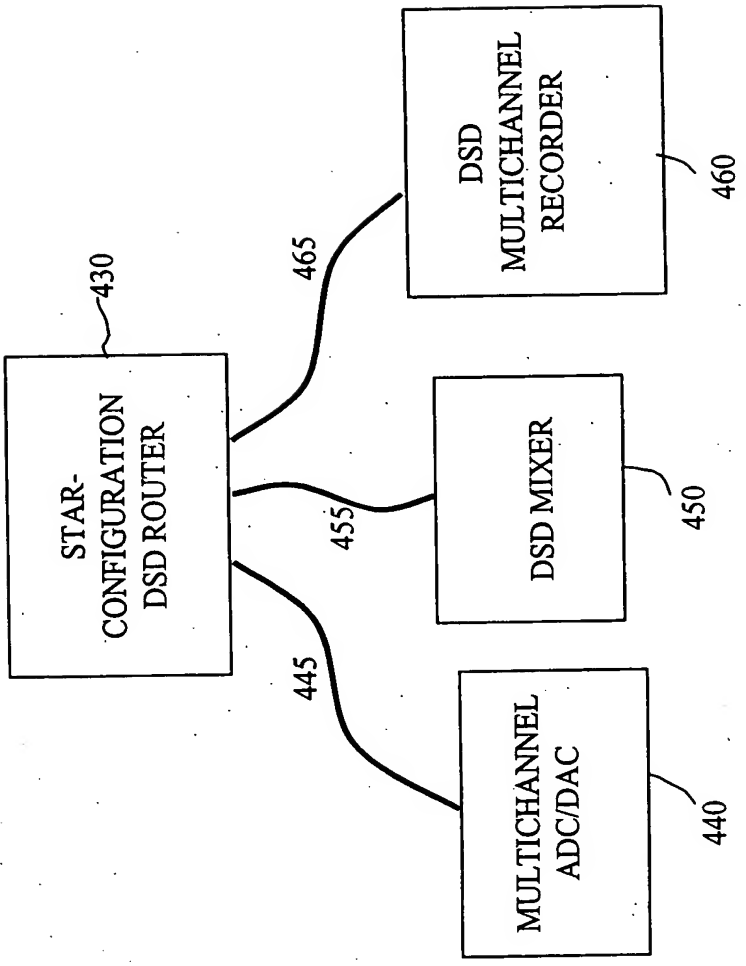

STAR-
CONFIGURATION
DSD ROUTER
430
465
DSD
MULTICHANNEL
RECORDER
460
455
DSD MIXER
450
445
MULTICHANNEL
ADC/DAC
440

FIGURE 4

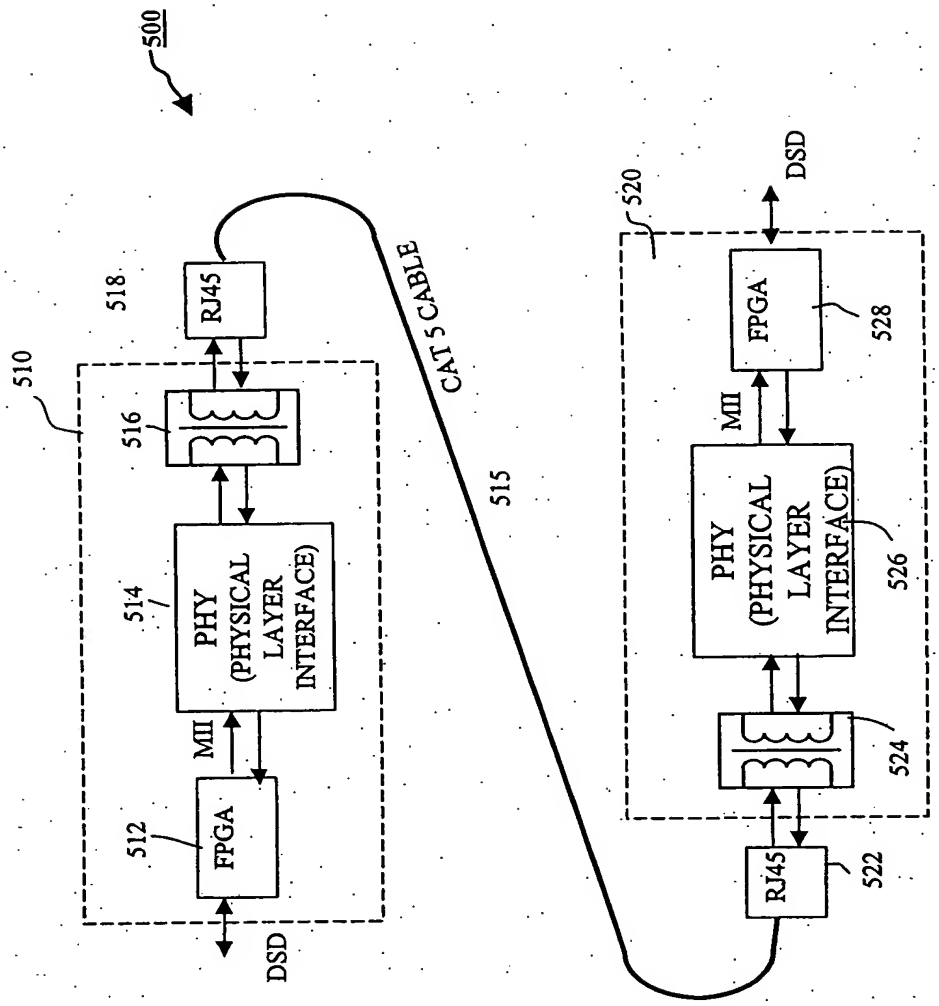

500
510
518
RJ45
516
514
PHY
(PHYSICAL
LAYER
INTERFACE)
MII
512
FPGA
DSD
CAT 5 CABLE
515
520
DSD
528
FPGA
MII
526
PHY
(PHYSICAL
LAYER
INTERFACE)
524
522
RJ45

FIGURE 5

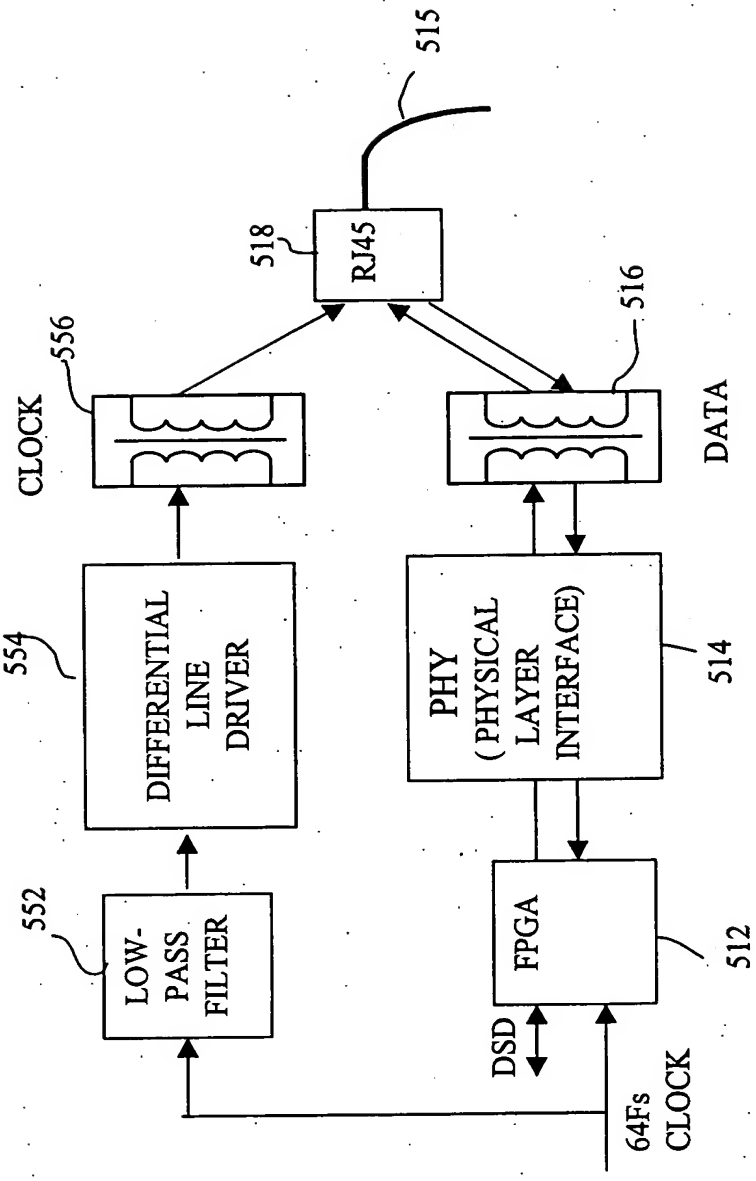

515
518
RJ45
516
556
CLOCK
DATA
554
DIFFERENTIAL LINE DRIVER
PHY (PHYSICAL LAYER INTERFACE)
514
552
LOW-PASS FILTER
FPGA
512
DSD
64Fs CLOCK

FIGURE 6

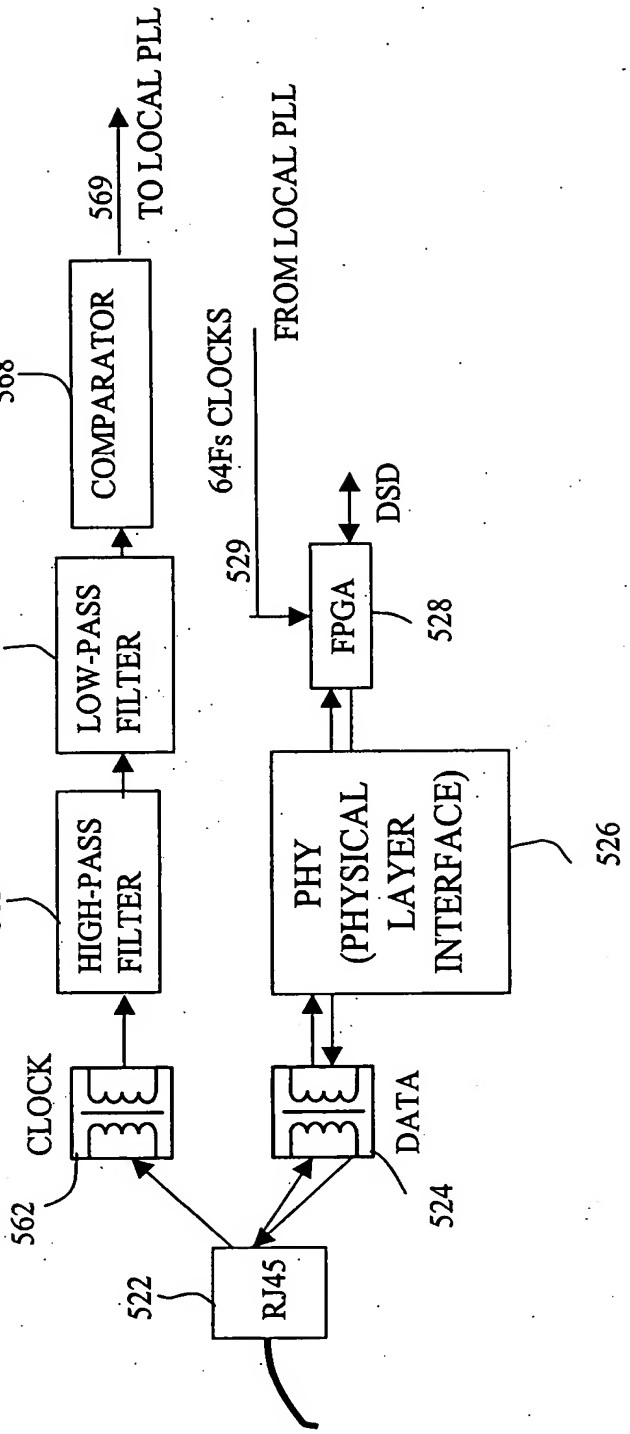

RJ45
522
CLOCK
562
DATA
524
HIGH-PASS FILTER
563
LOW-PASS FILTER
564
COMPARATOR
568
569
TO LOCAL PLL
PHY (PHYSICAL LAYER INTERFACE)
526
FPGA
528
DSD
64Fs CLOCKS
529
FROM LOCAL PLL

FIGURE 7

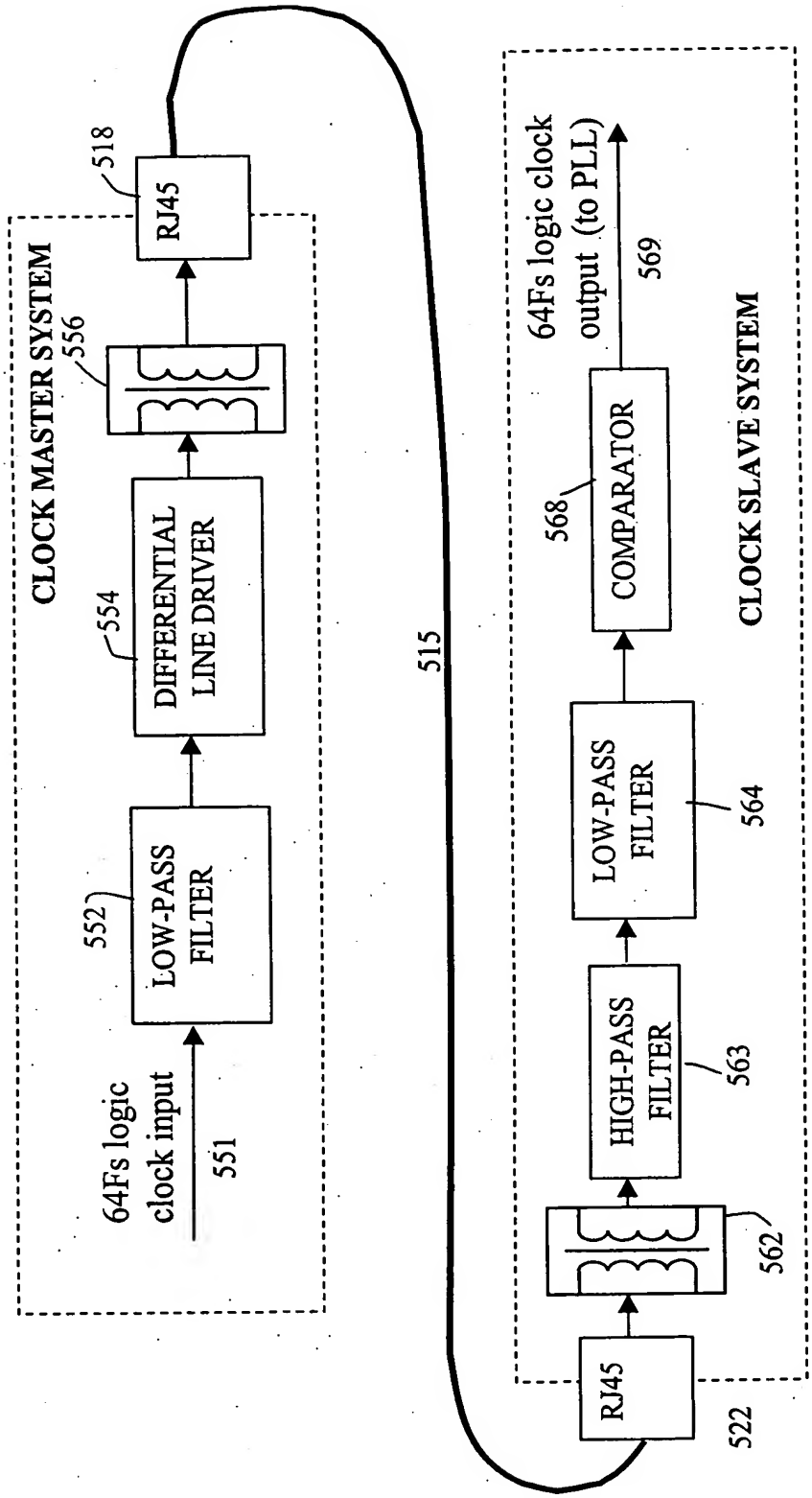

CLOCK MASTER SYSTEM
64Fs logic clock input
551
552
LOW-PASS FILTER
554
DIFFERENTIAL LINE DRIVER
556
518
RJ45
515
522
RJ45
562
HIGH-PASS FILTER
563
LOW-PASS FILTER
564
568
COMPARATOR
64Fs logic clock output (to PLL)
569
CLOCK SLAVE SYSTEM

FIGURE 8

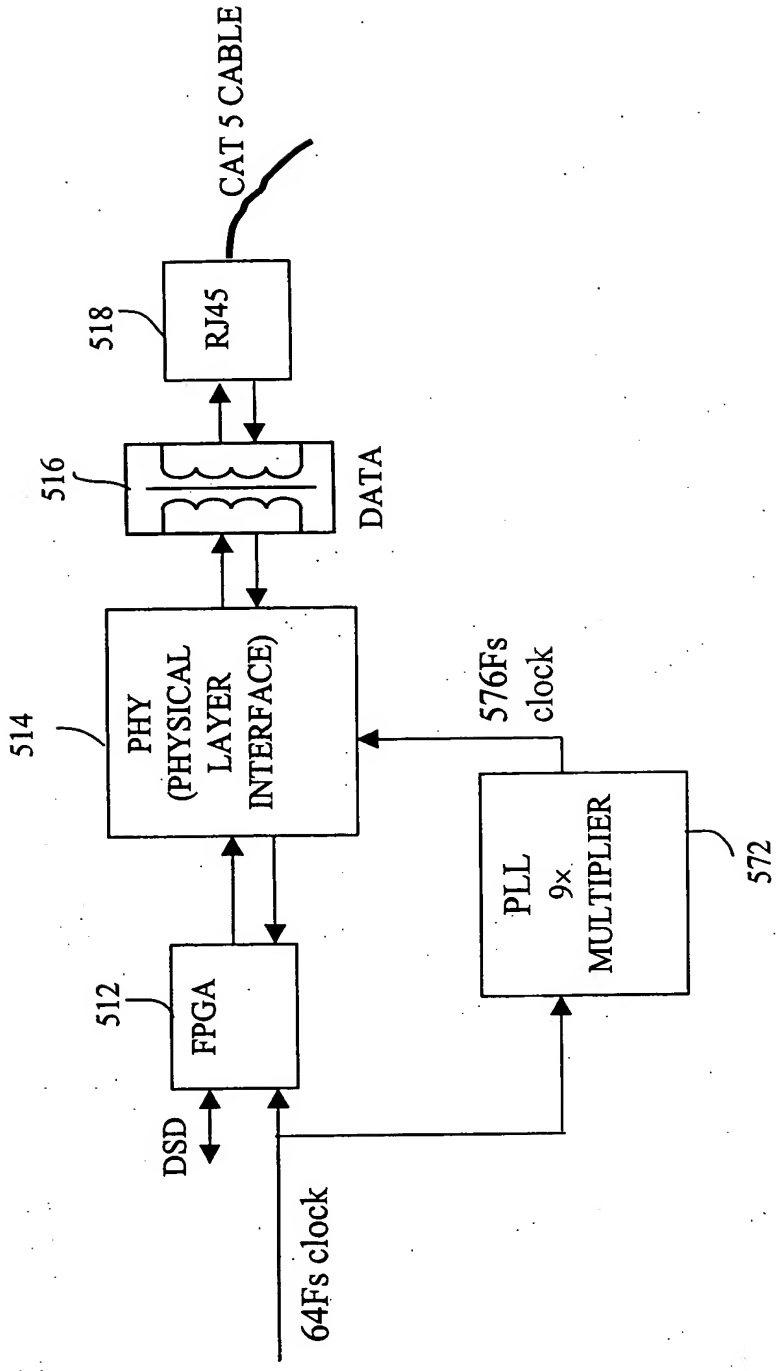

CAT 5 CABLE
518
RJ45
516
DATA
514
PHY
(PHYSICAL
LAYER
INTERFACE)
576Fs
clock
PLL
9x
MULTIPLIER
572
512
FPGA
DSD
64Fs clock

FIGURE 9

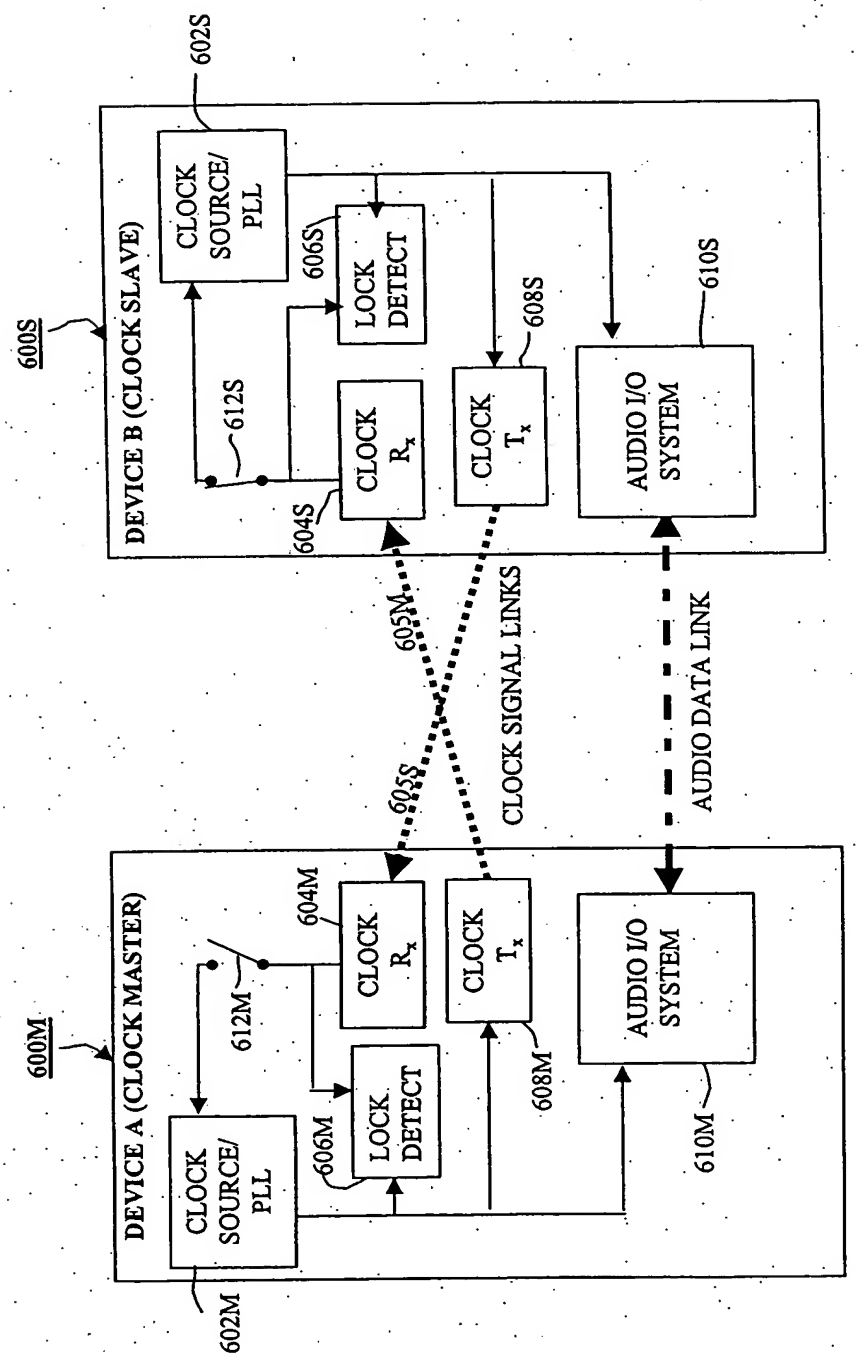

600S
DEVICE B (CLOCK SLAVE)
602S
CLOCK SOURCE/ PLL
606S
LOCK DETECT
612S
604S
CLOCK R_x
CLOCK T_x
608S
AUDIO I/O SYSTEM
610S
605M
605S
CLOCK SIGNAL LINKS
AUDIO DATA LINK
600M
DEVICE A (CLOCK MASTER)
604M
CLOCK R_x
CLOCK T_x
612M
606M
LOCK DETECT
608M
AUDIO I/O SYSTEM
610M
CLOCK SOURCE/ PLL
602M

FIGURE 10

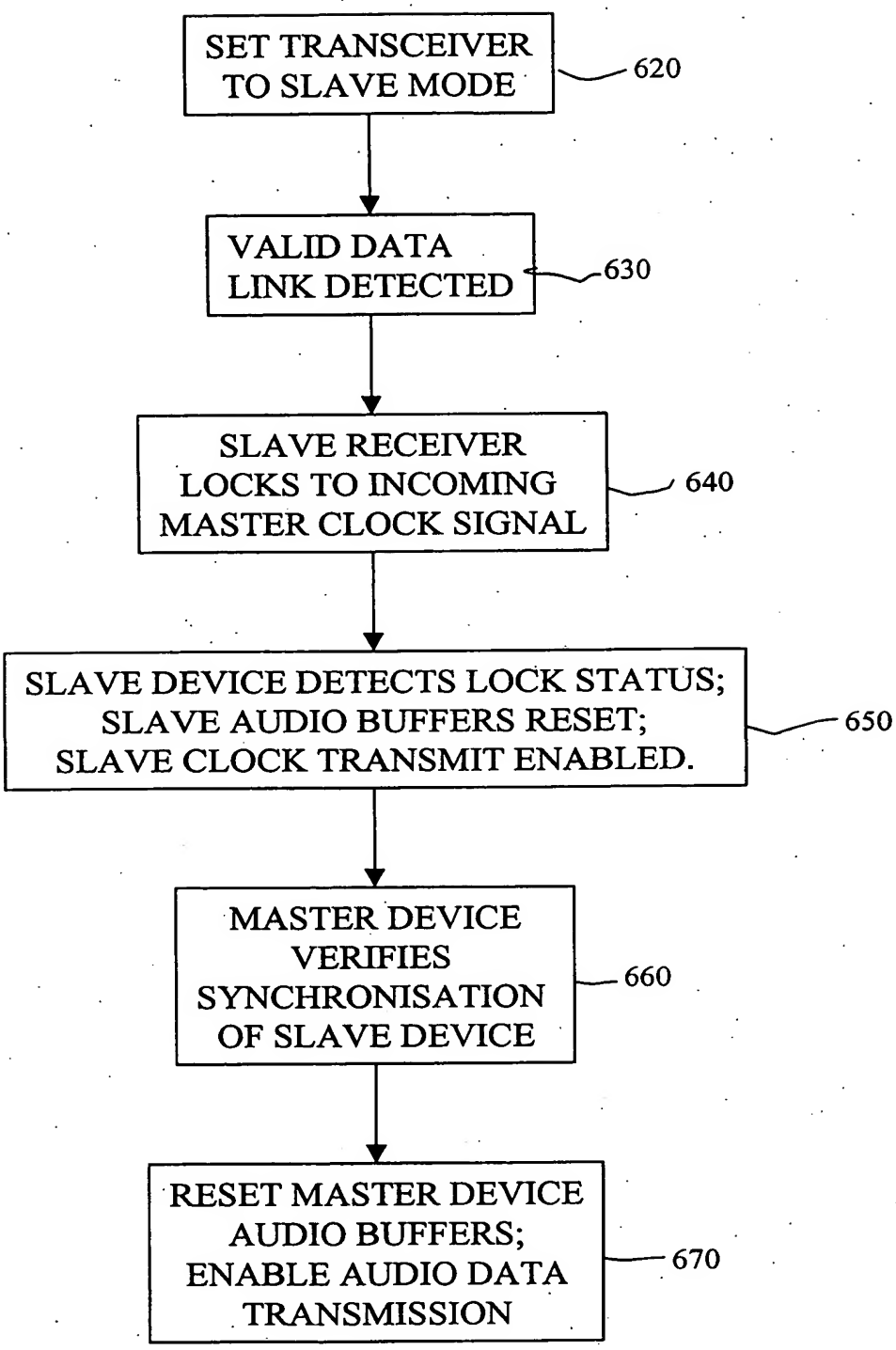

SET TRANSCEIVER TO SLAVE MODE
620
VALID DATA LINK DETECTED
630
SLAVE RECEIVER LOCKS TO INCOMING MASTER CLOCK SIGNAL
640
SLAVE DEVICE DETECTS LOCK STATUS; SLAVE AUDIO BUFFERS RESET; SLAVE CLOCK TRANSMIT ENABLED.
650
MASTER DEVICE VERIFIES SYNCHRONISATION OF SLAVE DEVICE
660
RESET MASTER DEVICE AUDIO BUFFERS; ENABLE AUDIO DATA TRANSMISSION
670

FIGURE 11

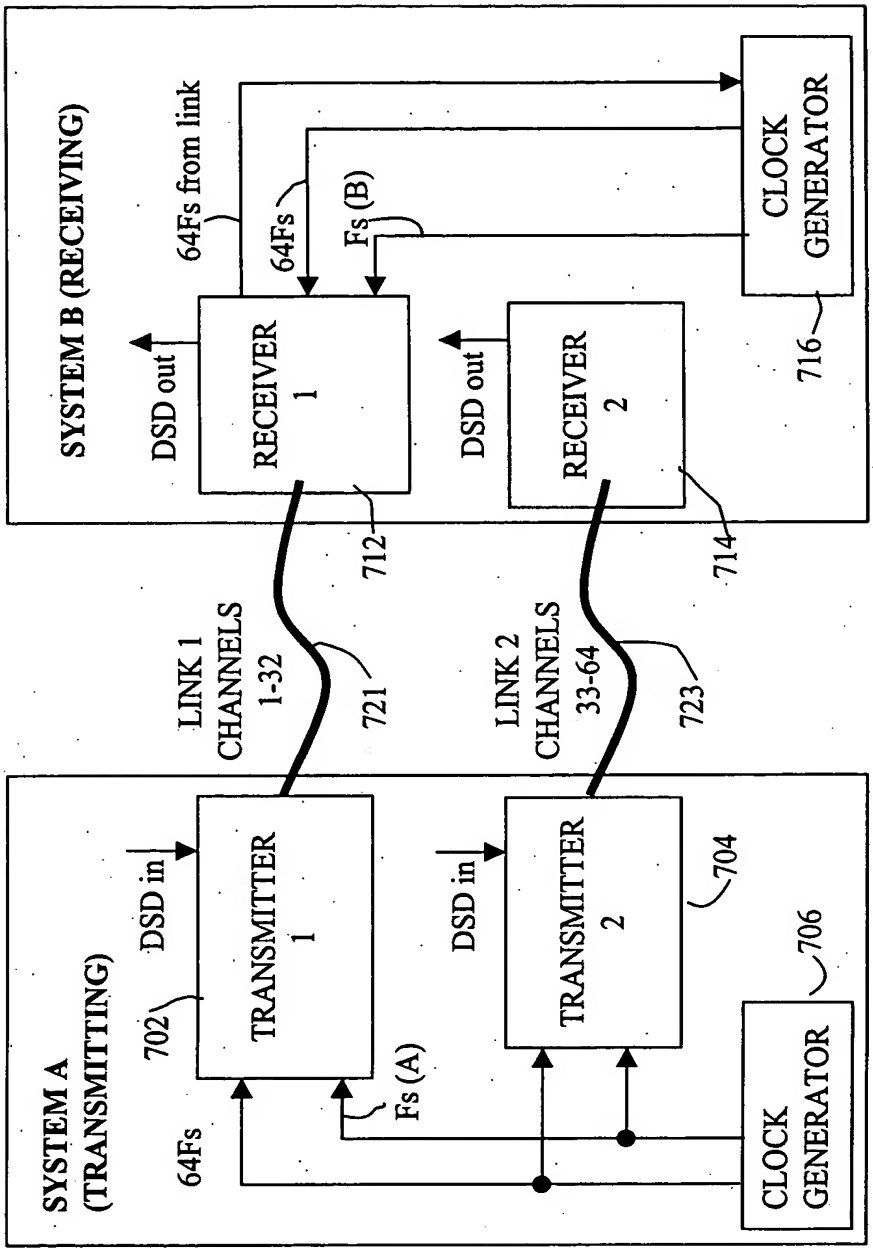

700A
700B
SYSTEM A
(TRANSMITTING)
SYSTEM B (RECEIVING)
DSD in
TRANSMITTER 1
TRANSMITTER 2
DSD out
RECEIVER 1
RECEIVER 2
64Fs
Fs (A)
64Fs from link
64Fs
Fs (B)
CLOCK GENERATOR
CLOCK GENERATOR
LINK 1 CHANNELS 1-32
LINK 2 CHANNELS 33-64
702
704
706
712
714
716
721
723

FIGURE 12

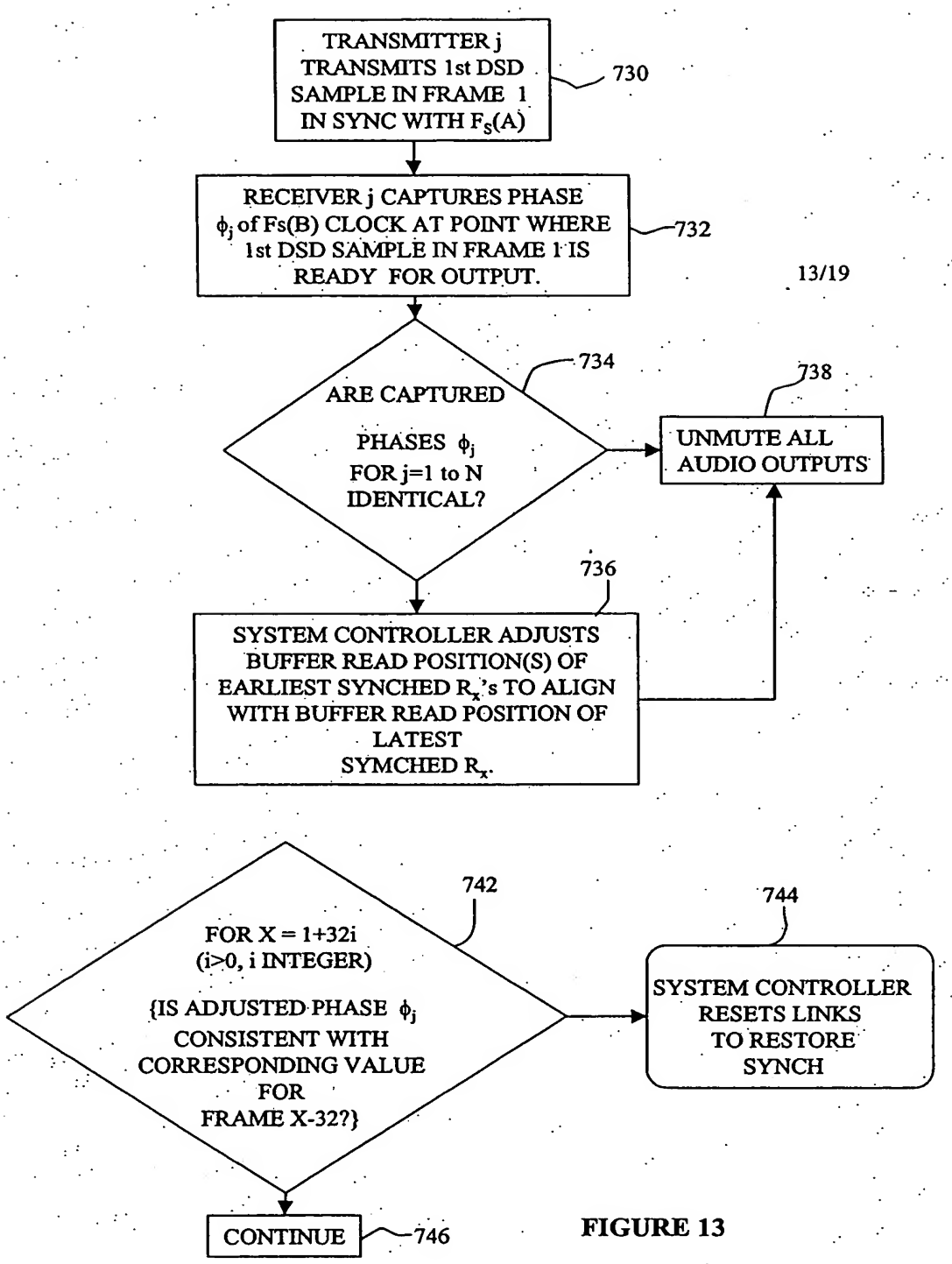

TRANSMITTER j TRANSMITS 1st DSD SAMPLE IN FRAME 1 IN SYNC WITH $F_S(A)$
730
RECEIVER j CAPTURES PHASE ϕ_j of Fs(B) CLOCK AT POINT WHERE 1st DSD SAMPLE IN FRAME 1 IS READY FOR OUTPUT.
732
13/19
ARE CAPTURED PHASES ϕ_j FOR j=1 to N IDENTICAL?
734
738
UNMUTE ALL AUDIO OUTPUTS
736
SYSTEM CONTROLLER ADJUSTS BUFFER READ POSITION(S) OF EARLIEST SYNCHED R_x's TO ALIGN WITH BUFFER READ POSITION OF LATEST SYMCHED R_x.
FOR X = 1+32i (i>0, i INTEGER) {IS ADJUSTED PHASE ϕ_j CONSISTENT WITH CORRESPONDING VALUE FOR FRAME X-32?}
742
744
SYSTEM CONTROLLER RESETS LINKS TO RESTORE SYNCH
CONTINUE
746

FIGURE 13

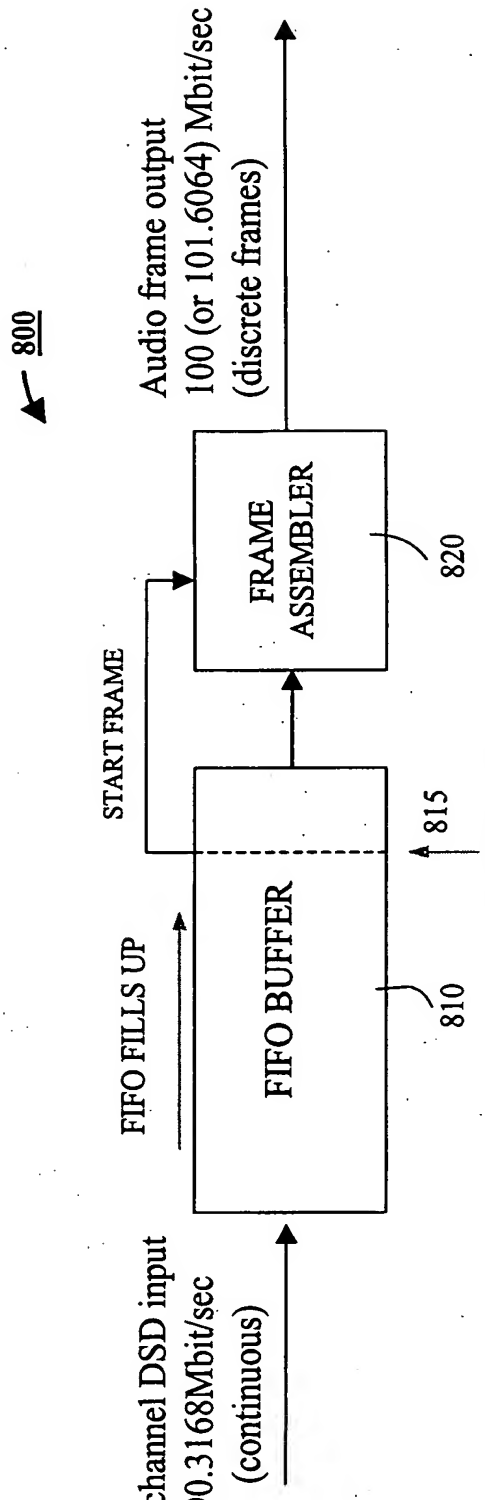

800
32-channel DSD input
90.3168Mbit/sec
(continuous)
FIFO FILLS UP
FIFO BUFFER
810
815
THRESHOLD
LEVEL
START FRAME
FRAME
ASSEMBLER
820
Audio frame output
100 (or 101.6064) Mbit/sec
(discrete frames)

FIGURE 14

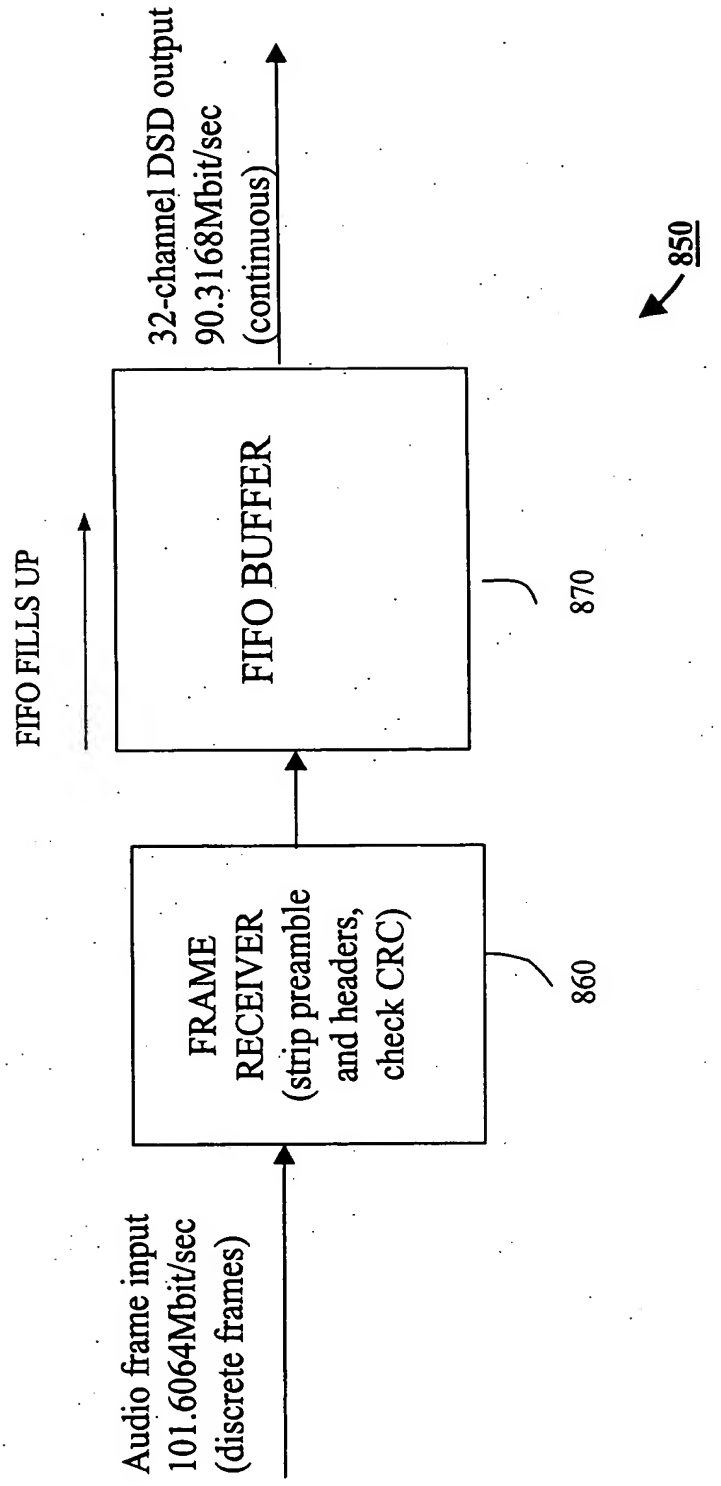
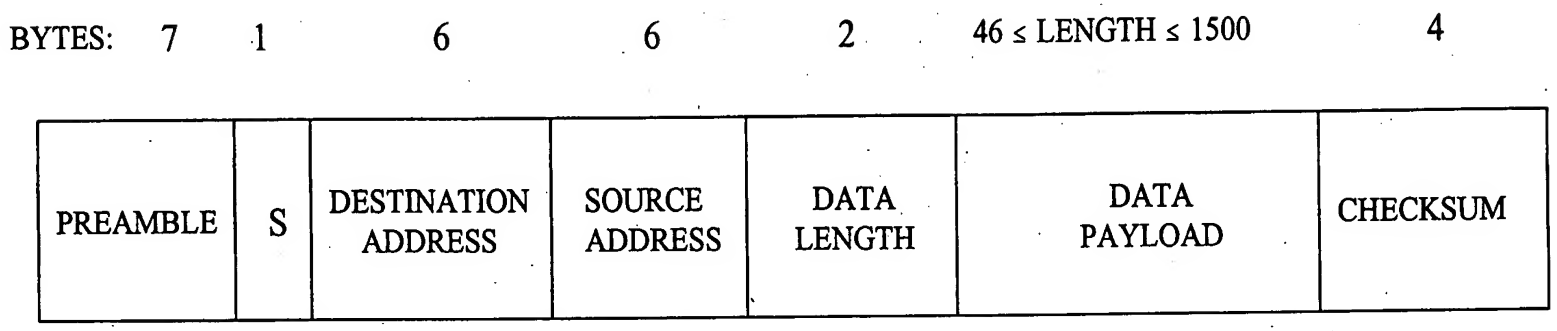
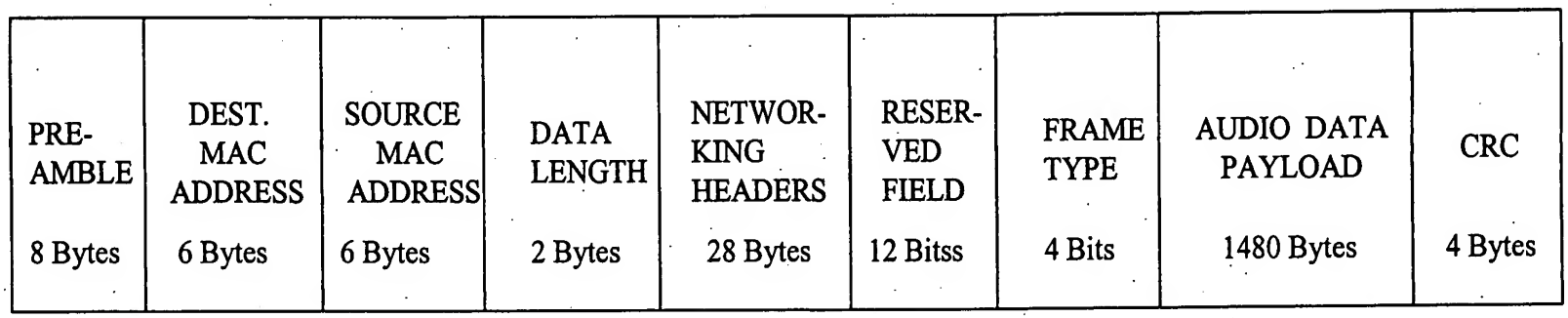

Audio frame input
101.6064Mbit/sec
(discrete frames)
FRAME
RECEIVER
(strip preamble
and headers,
check CRC)
860
FIFO BUFFER
870
FIFO FILLS UP
32-channel DSD output
90.3168Mbit/sec
(continuous)
850

FIGURE 15



STANDARD ETHERNET FRAME

FIGURE 16



AUDIO DATA FRAME

FIGURE 17

AUDIO DATA FRAME

Word	B31-B28	B27-B24	B23-B20	B19-B16	B15-B12	B11-B8	B7-B4	B3-B0
0	5h	5h	5h	5h	5h	5h	5h	5h
1	Dh	5h	5h	5h	5h	5h	5h	5h
2	Reserved for destination MAC address							
3	Reserved for source MAC address				Reserved for dest. MAC address			
4	Reserved for source MAC address							
5					Length - always 1510 bytes (0x5E6)			
6								
7								
8	Reserved for networking headers							
9								
10								
11								
12	reserved	reserved	reserved	frame type				
13-382	370 samples 32-channel DSD audio							
383	CRC							

FIGURE 18A

Word	B31-B28	B27-B24	B23-B20	B19-B16	B15-B12	B11-B8	B7-B4	B3-B0
0	5h	5h	5h	5h	5h	5h	5h	5h
1	Dh	5h	5h	5h	5h	5h	5h	5h
2	Reserved for destination MAC address							
3	Reserved for source MAC address				Reserved for destination MAC address			
4	Reserved for source MAC address							
5	IP Type of Service		IP Hdr Lnth	IP Version	Length – 1446 bytes (0x05A6)			
6	IP Datagram ID				IP Datagram Length			
7	IP Protocol		IP TTL		IP Fragment Offset			IP Flgs
8	Source IP Address (low 16)				IP Header Checksum			
9	Destination IP Address (low 16)				Source IP Address (high 16)			
10	IP Options (low 16)				Destination IP Address (high 16)			
11	UDP Source Port				IP Header Padding		IP Options (high 8)	
12	UDP Length				UDP Destination Port			
13	Frame format ID (0)				UDP Checksum			
14	Frame format ID (2)				Frame format ID (1)			
15-366	1408-byte frame payload (352 DSD samples, 24 channels, plus 88 bytes aux data)							
367	CRC							

Fig 18B

CONTROL DATA FRAME

Word	B31-B28	B27-B24	B23-B20	B19-B16	B15-B12	B11-B8	B7-B4	B3-B0
0	5h	5h	5h	5h	5h	5h	5h	5h
1	Dh	5h	5h	5h	5h	5h	5h	5h
2	Reserved for destination MAC address							
3	Reserved for source MAC address				Reserved for dest. MAC address			
4	Reserved for source MAC address							
5					Length			
6								
7								
8	Reserved for networking headers							
9								
10								
11								
12	reserved	reserved	reserved	frame type				
13-24	48 bytes control data (of arbitrary format)							
25	CRC							

FIGURE 19

Bits 15:12	Bits 11:8	Bits 7:4	Bits 3:0
Flags	Frame Type	Protocol Major Ver.	Protocol Minor Ver.

Fig. 20

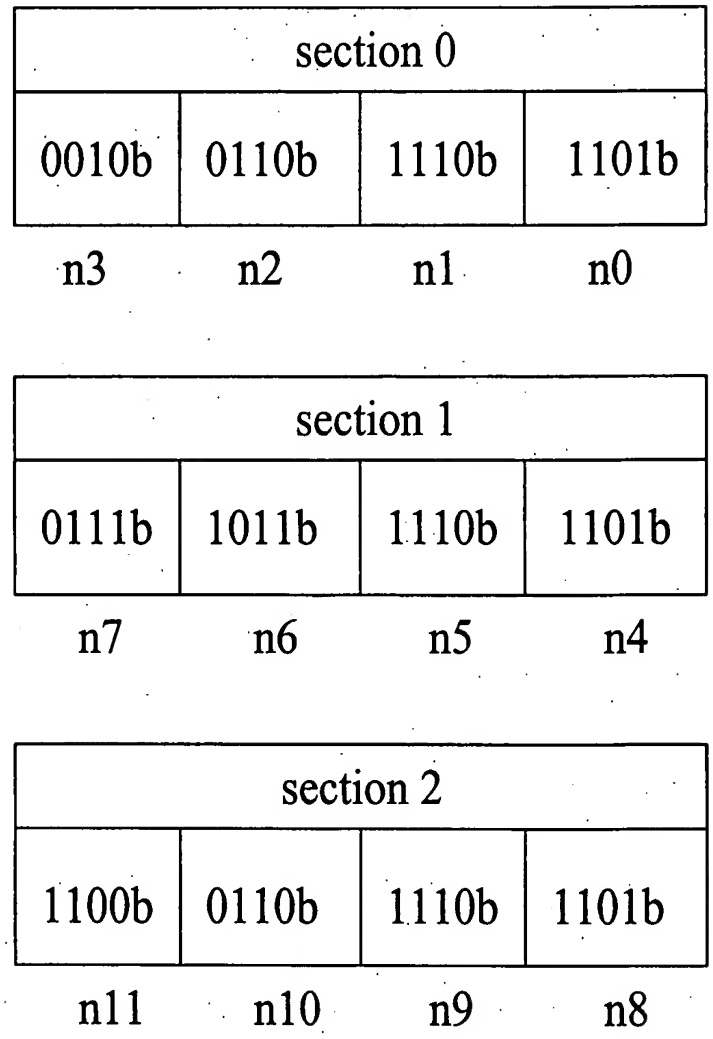

section 0
0010b
0110b
1110b
1101b
n3
n2
n1
n0
Word 13 bits 16-31
section 1
0111b
1011b
1110b
1101b
n7
n6
n5
n4
Word 14 bits 0-15
section 2
1100b
0110b
1110b
1101b
n11
n10
n9
n8
Word 14 bits 16-31

Fig. 21

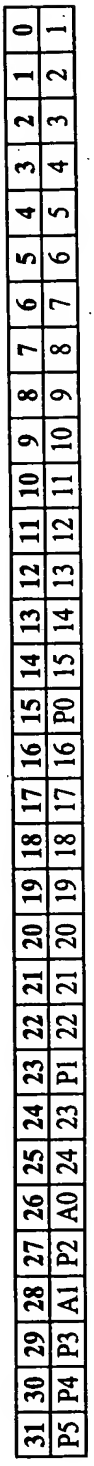

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
P5 P4 P3 A1 P2 A0 24 23 P1 22 21 20 19 18 17 16 P0 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Fig. 22

Parity bit	Data block elements XNOR'd to generate parity bit														
P0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
P1	1	2	3	4	5	6	7	8	16	17	18	19	20	21	22
P2	1	2	3	4	9	10	11	12	16	17	18	19	23	24	A0
P3	1	2	5	6	9	10	13	14	16	17	20	21	23	24	A1
P4	1	3	5	7	9	11	13	15	16	18	20	22	23	A0	A1
P5	(all elements – global parity bit)														

FIGURE 23A

Syndrome bit	Data block elements XOR'd to generate syndrome bit															
s_0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	P0
s_1	1	2	3	4	5	6	7	8	16	17	18	19	20	21	22	P1
s_2	1	2	3	4	9	10	11	12	16	17	18	19	23	24	A0	P2
s_3	1	2	5	6	9	10	13	14	16	17	20	21	23	24	A1	P3
s_4	1	3	5	7	9	11	13	15	16	18	20	22	23	A0	A1	P4
s_5	(all elements including parity bits)															

FIGURE 23B

Nibble	Bit 3	Bit 2	Bit 1	Bit 0
0	B3[0]	B2[0]	B1[0]	B0[0]
1	B7[0]	B6[0]	B5[0]	B4[0]
2	B11[0]	B10[0]	B9[0]	B8[0]
...	...	...	...	...
7	B31[0]	B30[0]	B29[0]	B28[0]
8	B3[1]	B2[1]	B1[1]	B0[1]
9	B7[1]	B6[1]	B5[1]	B4[1]
...	...	...	...	...
254	B27[31]	B26[31]	B25[31]	B24[31]
255	B31[31]	B30[31]	B29[31]	B28[31]
256	B35[0]	B34[0]	B33[0]	B32[0]
257	B39[0]	B38[0]	B37[0]	B36[0]
...	...	...	...	...
2814	B347[31]	B346[31]	B345[31]	B344[31]
2815	B351[31]	B350[31]	B349[31]	B348[31]

Fig 24

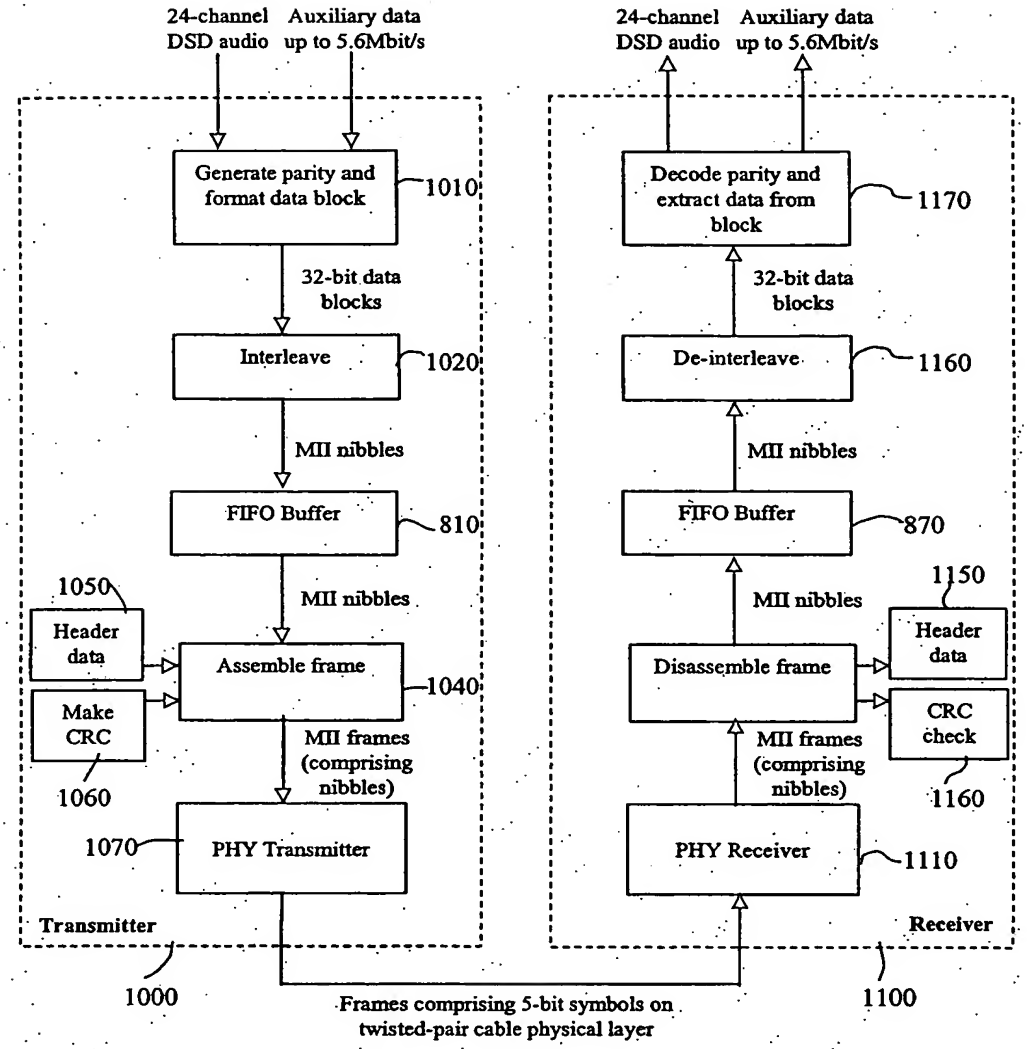

24-channel DSD audio
Auxiliary data up to 5.6Mbit/s
Generate parity and format data block
1010
32-bit data blocks
Interleave
1020
MII nibbles
FIFO Buffer
810
1050
Header data
MII nibbles
Assemble frame
1040
Make CRC
1060
MII frames (comprising nibbles)
1070
PHY Transmitter
Transmitter
1000
24-channel DSD audio
Auxiliary data up to 5.6Mbit/s
Decode parity and extract data from block
1170
32-bit data blocks
De-interleave
1160
MII nibbles
FIFO Buffer
870
1150
MII nibbles
Header data
Disassemble frame
CRC check
MII frames (comprising nibbles)
1160
PHY Receiver
1110
Receiver
1100
Frames comprising 5-bit symbols on twisted-pair cable physical layer

Fig. 25

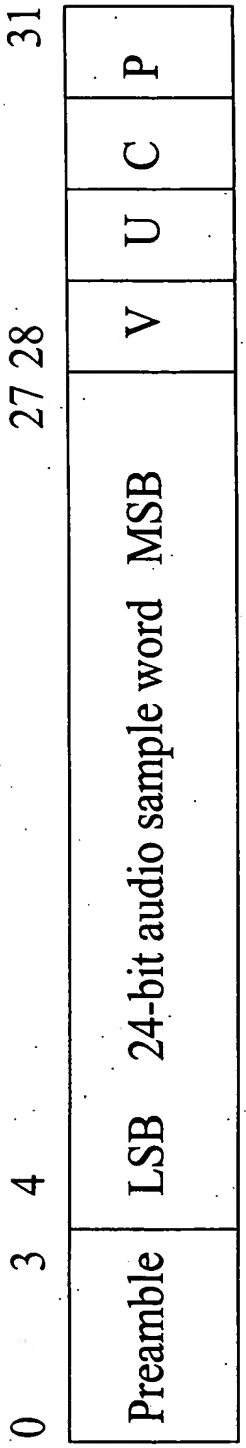


Fig 26A

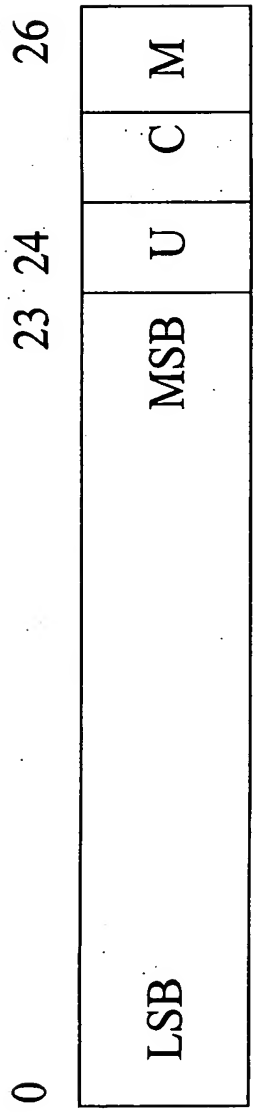


Fig 26B

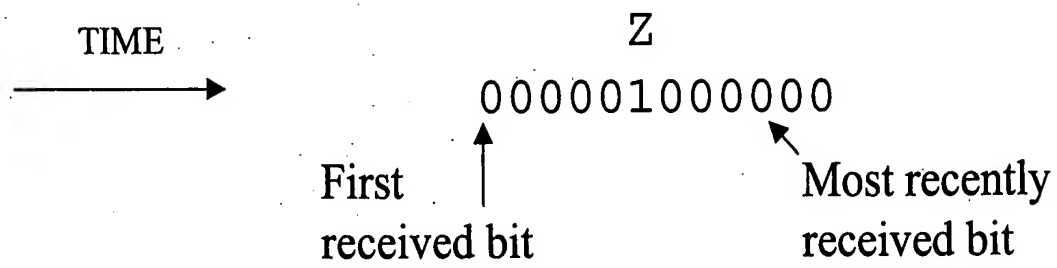


Fig. 27A

S

0000000011...

Fig. 27B

SV

0000000011100000

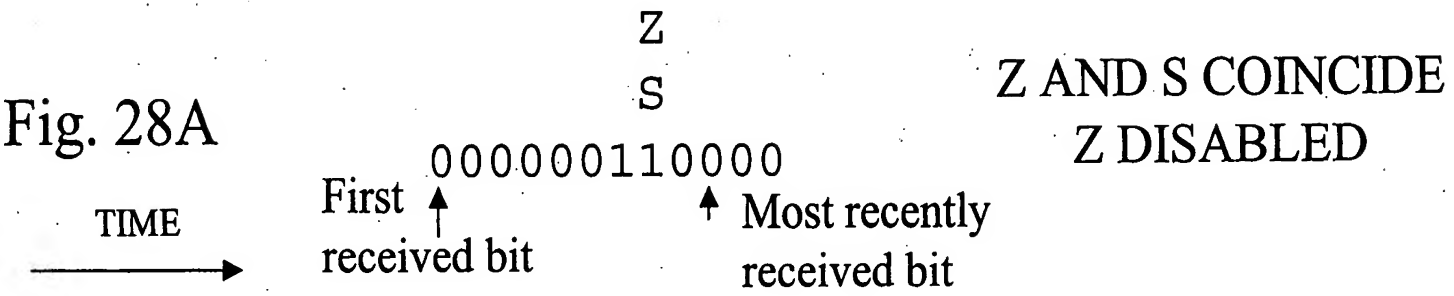
Fig. 27C

SV

0000000011000000

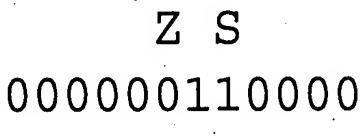
Fig. 27D

Fig. 28A



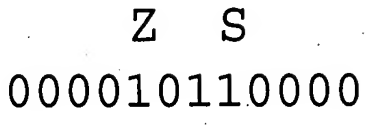
Z AND S COINCIDE
Z DISABLED

Fig. 28B



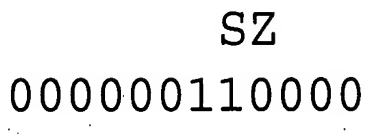
Z IMMEDIATELY PRECEDES S
SO Z DISABLED

Fig. 28C



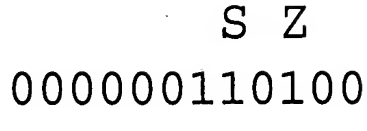
Z ENABLED

Fig. 28D



Z IMMEDIATELY FOLLOWS S
SO Z DISABLED

Fig. 28E



Z ENABLED

Type value	Frame format
0x0	64fs DSD (as Protocol Spec v1.1)
0x1	Reserved
0x2	Reserved
0x3	Reserved
0x4	PCM, 4 sample sub-frames
0x5	PCM, 5 sample sub-frames
0x6	PCM, 6 sample sub-frames
0x7	PCM, 7 sample sub-frames
0x8	PCM, 8 sample sub-frames
0x9	PCM, 9 sample sub-frames
0xA	PCM, 10 sample sub-frames
0xB	PCM, 11 sample sub-frames
0xC	PCM, 12 sample sub-frames
0xD	PCM, 13 sample sub-frames
0xE	Reserved
0xF	Reserved

Fig 29

Flag bit	Name	Description
0	44.1kHz sync flag	1: First DSD sample in frame was received at transmitter simultaneously with 44.1kHz sync clock positive edge 0: First DSD sample in frame was **not** received at transmitter simultaneously with 44.1kHz sync clock positive edge
1	fs/n sync flag	1: First DSD sample in frame was received at transmitter simultaneously with fs/n sync clock positive edge 0: First DSD sample in frame was **not** received at transmitter simultaneously with fs/n sync clock positive edge
others	(not used)	Set to 0 by transmitter, ignored by receiver

Fig 30

(Type field = 0x4 through 0xD, PCM)

Flag bits	Name	Description
1:0	Clock base flag	00: 44.1kHz (+/-100ppm) audio base clock 01: 48kHz (+/-100ppm) audio base clock 10: Varispeed (38.5875kHz to 54kHz) audio base clock 11: (reserved)
3:2	Base clock sample rate multiplier	00: 1x base clock (f_s) 01: 2x base clock ($2f_s$) 10: 4x base clock ($4f_s$) 11: 8x base clock ($8f_s$)

Fig 31

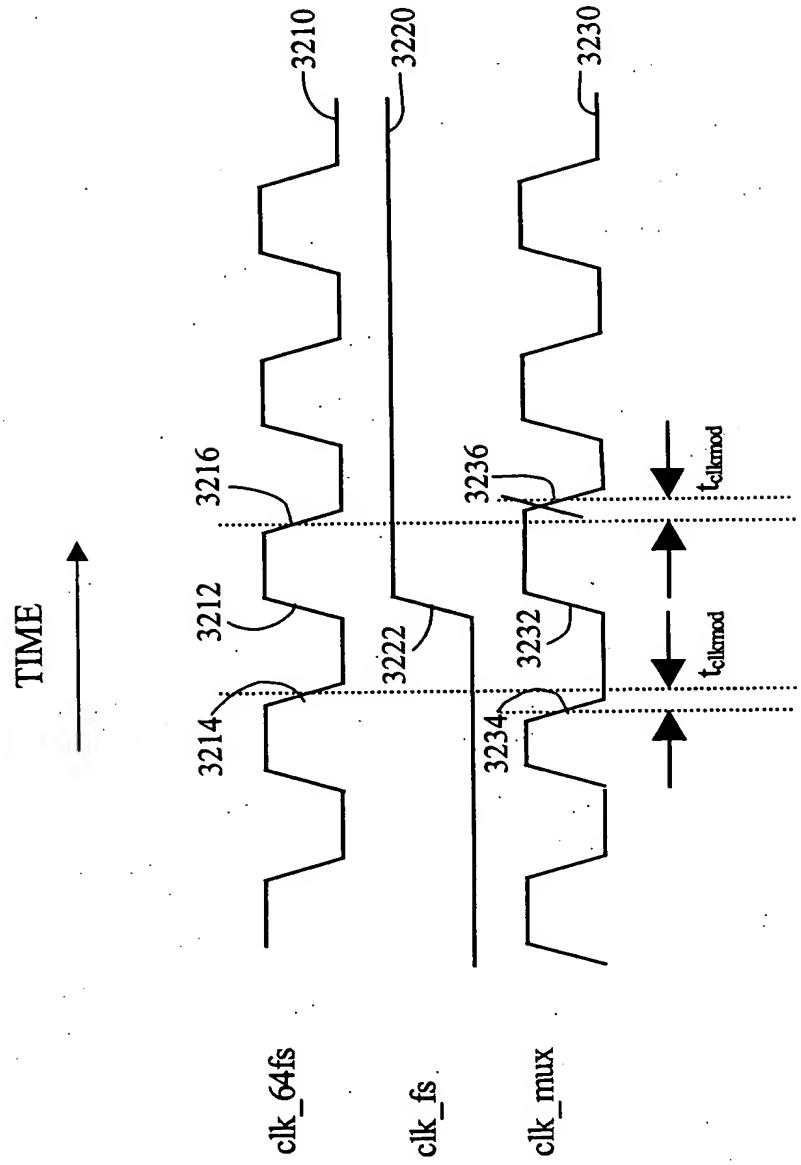

TIME
clk_64fs
clk_fs
clk_mux
3210
3220
3230
3212
3214
3216
3222
3232
3234
3236
t_{clkmod}
t_{clkmod}

Fig 32

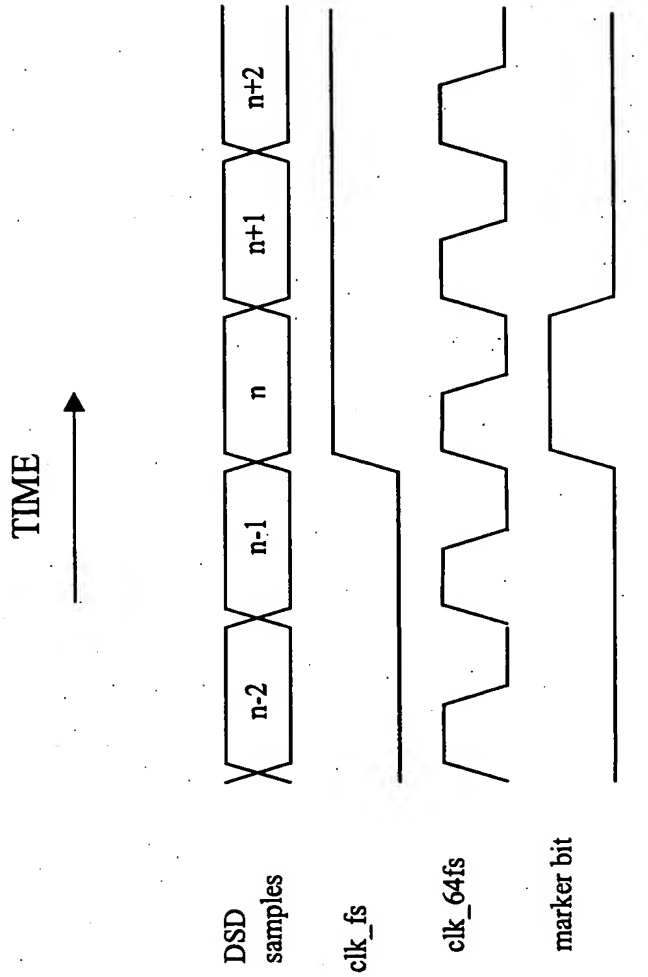


Fig 33

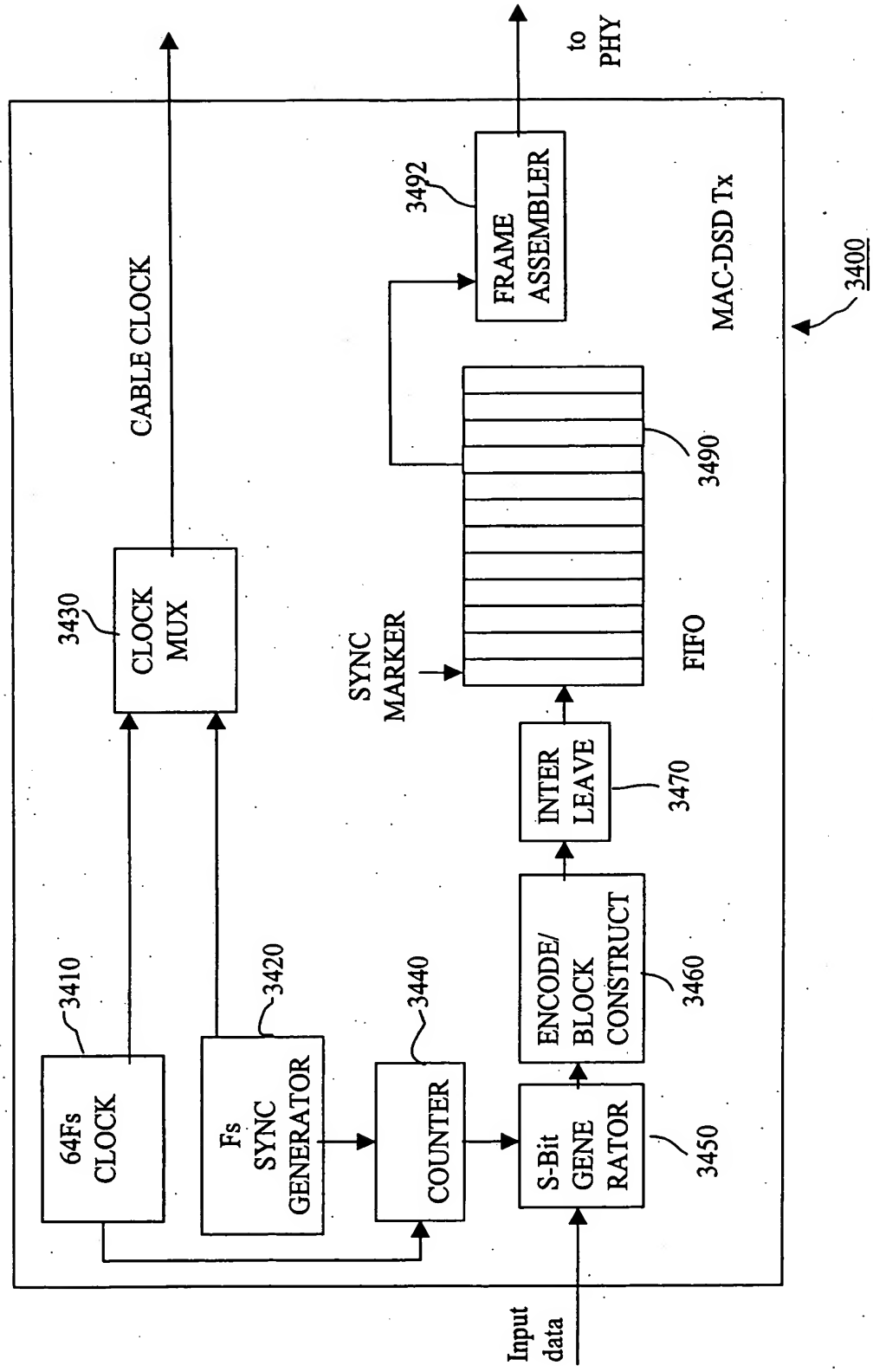

to PHY
CABLE CLOCK
3492
FRAME ASSEMBLER
MAC-DSD Tx
3400
3490
3430
CLOCK MUX
SYNC MARKER
FIFO
INTER LEAVE
3470
3410
64Fs CLOCK
3420
Fs SYNC GENERATOR
3440
COUNTER
ENCODE/ BLOCK CONSTRUCT
3460
S-Bit GENE RATOR
3450
Input data

Fig 34

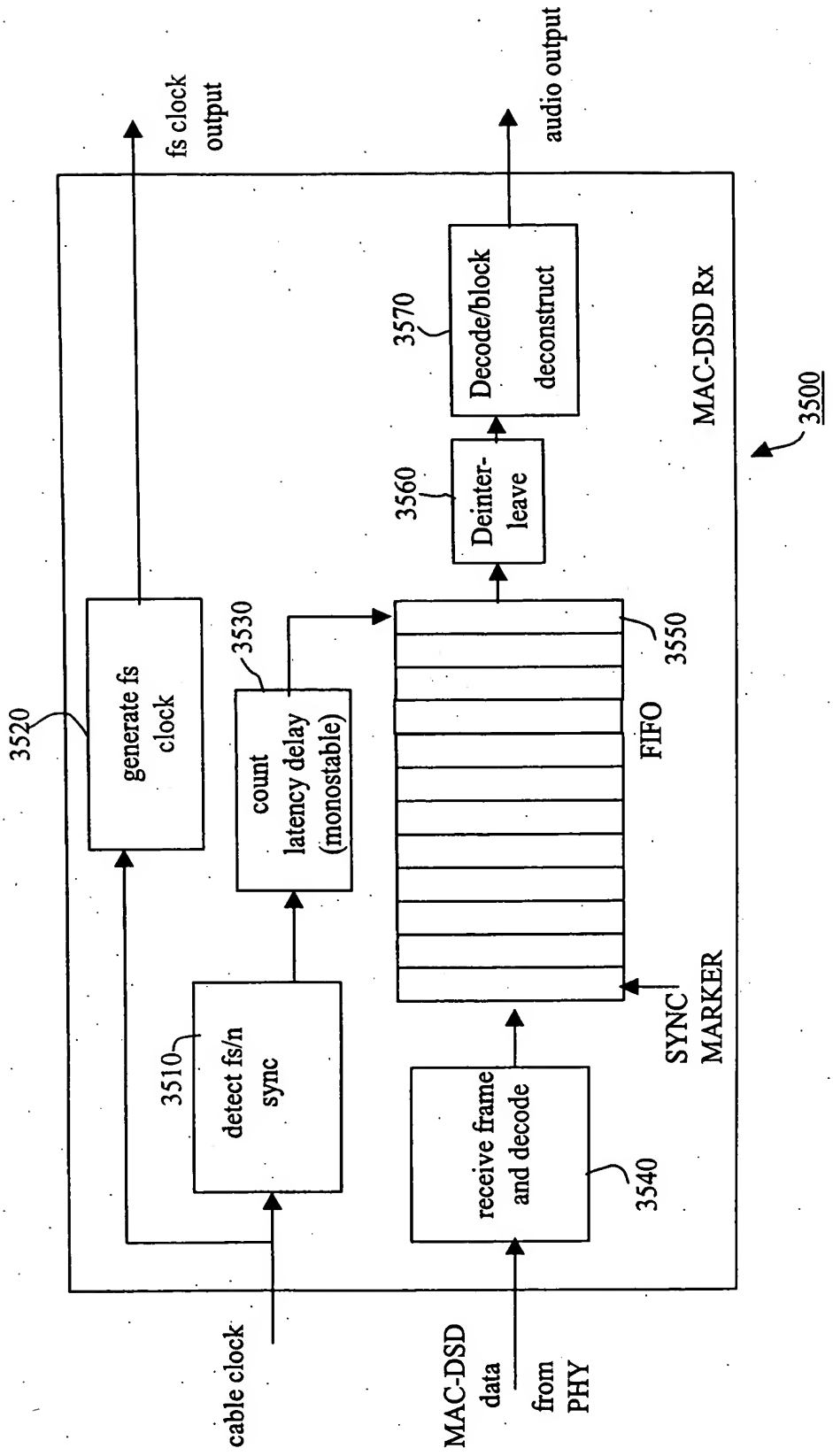

fs clock output
audio output
MAC-DSD Rx
3500
3570
Decode/block deconstruct
3560
Deinter-leave
3520
generate fs clock
3530
count latency delay (monostable)
3550
FIFO
3510
detect fs/n sync
SYNC MARKER
receive frame and decode
3540
cable clock
MAC-DSD data
from PHY

Fig 35

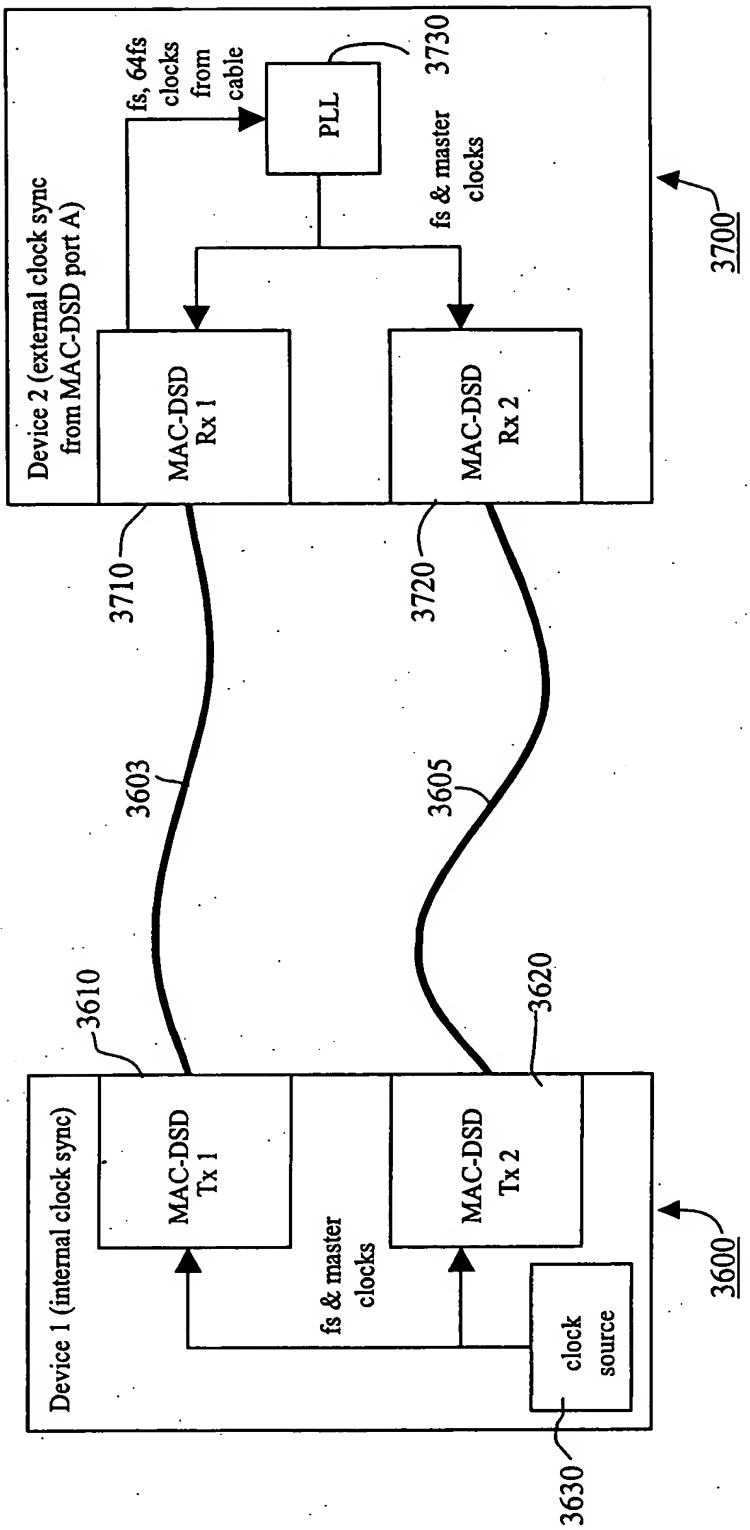

Device 2 (external clock sync from MAC-DSD port A)
fs, 64fs clocks from cable
PLL
3730
fs & master clocks
MAC-DSD Rx 1
MAC-DSD Rx 2
3700
3710
3720
3603
3605
3610
3620
Device 1 (internal clock sync)
MAC-DSD Tx 1
MAC-DSD Tx 2
fs & master clocks
clock source
3600
3630

Fig 36

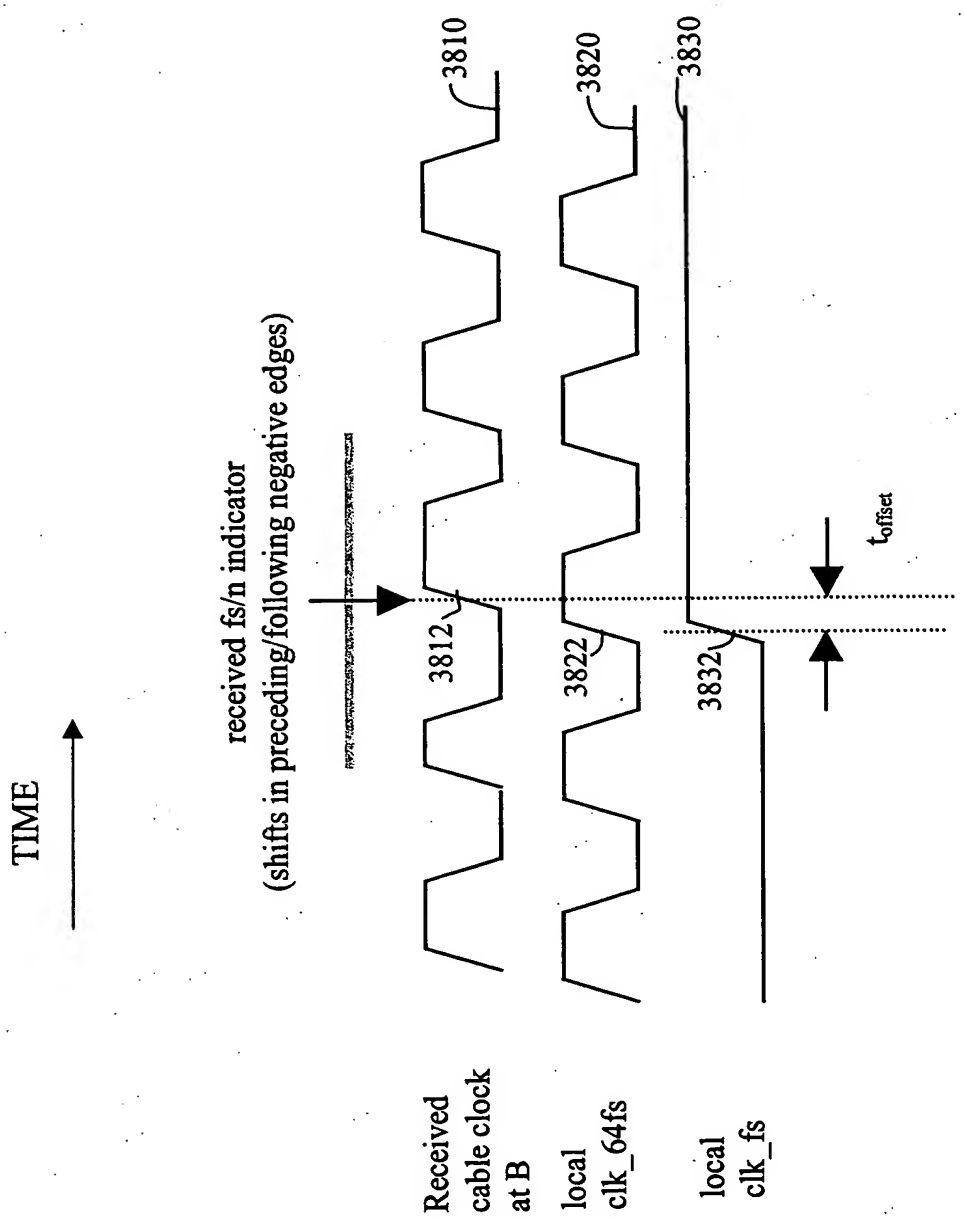

TIME
received fs/n indicator
(shifts in preceding/following negative edges)
Received cable clock at B
local clk_64fs
local clk_fs
3810
3820
3830
3812
3822
3832
t_{offset}

Fig 37

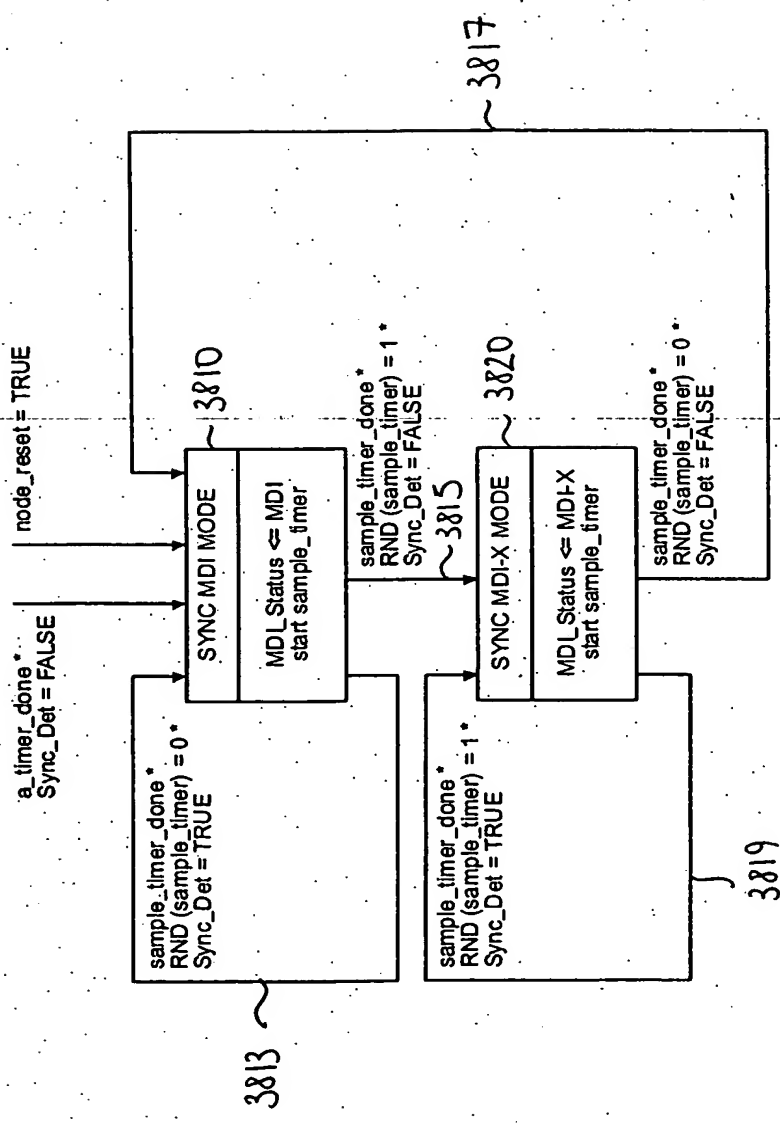

node_reset = TRUE
a_timer_done *
Sync_Det = FALSE
SYNC MDI MODE
MDI_Status <= MDI
start sample_timer
3810
sample_timer_done *
RND (sample_timer) = 1 *
Sync_Det = FALSE
3815
SYNC MDI-X MODE
MDI_Status <= MDI-X
start sample_timer
3820
sample_timer_done *
RND (sample_timer) = 0 *
Sync_Det = FALSE
3817
sample_timer_done *
RND (sample_timer) = 0 *
Sync_Det = TRUE
3813
sample_timer_done *
RND (sample_timer) = 1 *
Sync_Det = TRUE
3819

Fig 38

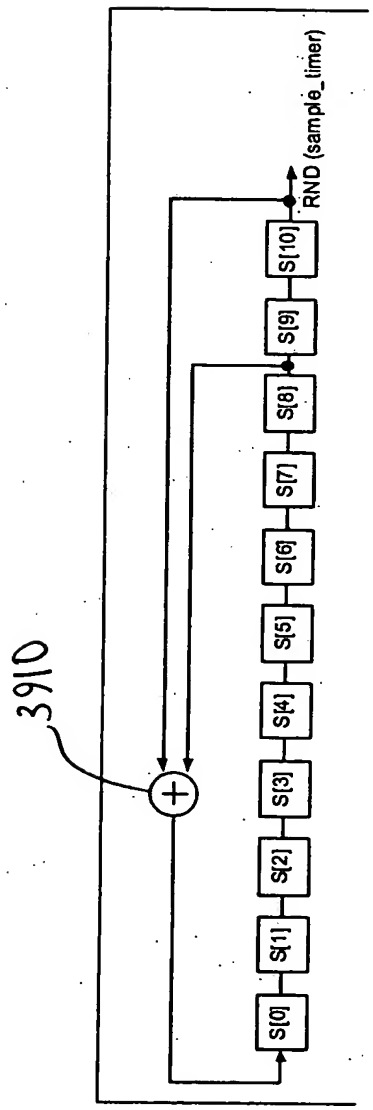


Fig 39

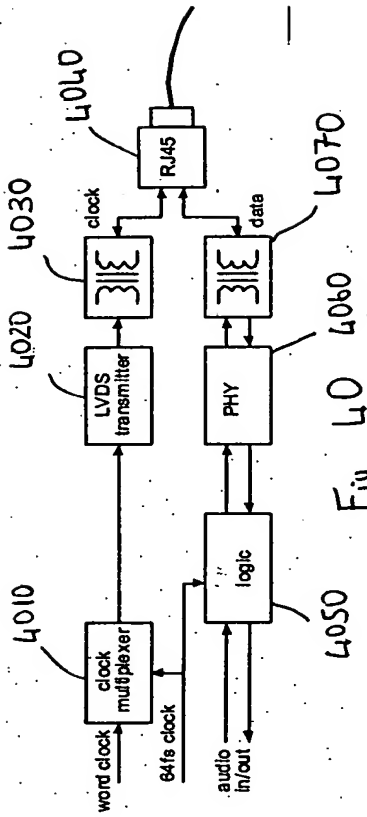

4040
RJ45
4030
clock
data
4070
4020
LVDS transmitter
PHY
4060
4010
clock multiplexer
logic
4050
word clock
64fs clock
audio in/out

Fig 40

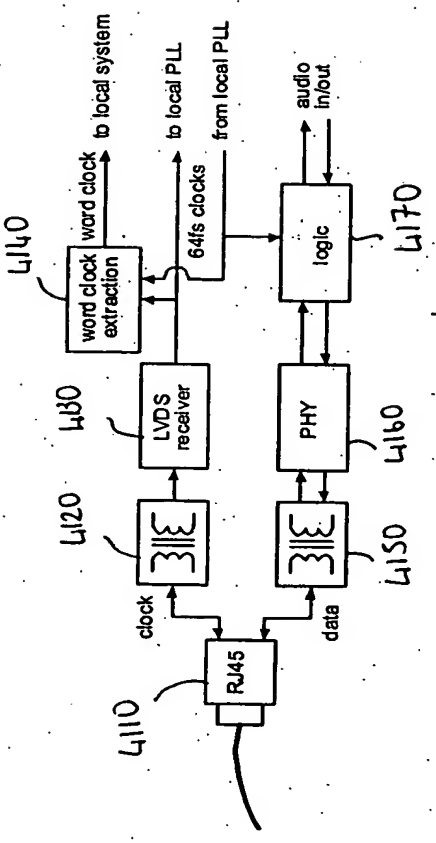

4140
word clock extraction
word clock
to local system
to local PLL
from local PLL
64fs clocks
audio in/out
4130
LVDS receiver
logic
4170
4120
PHY
4160
clock
data
4150
4110
RJ45

Fig 41

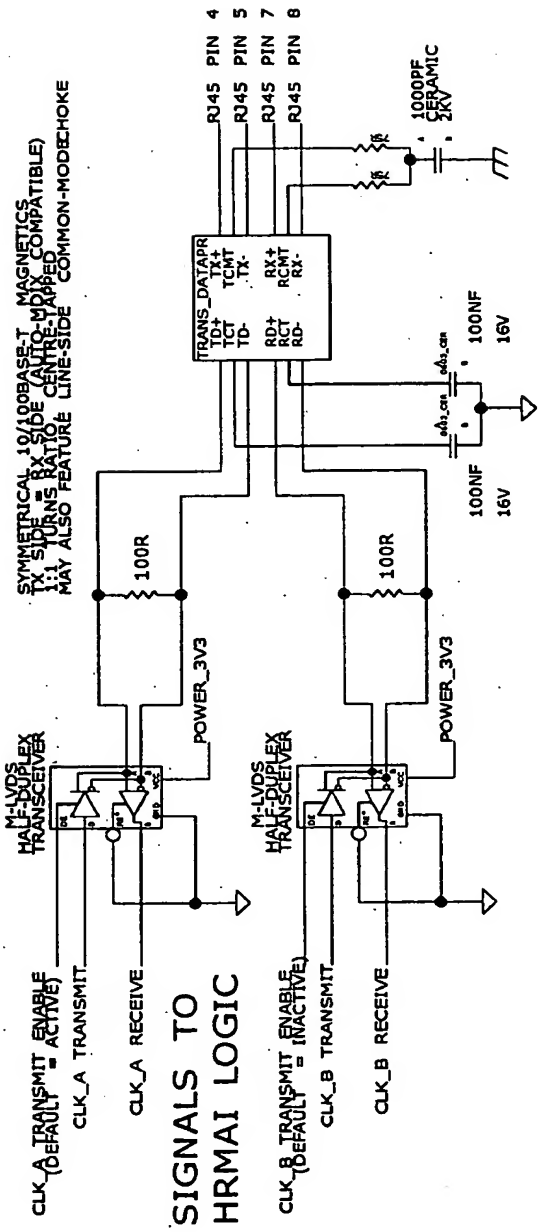

SYMMETRICAL 10/100BASE-T MAGNETICS
TX SIDE TURNS RATIO 1:1
RX SIDE CENTRE-TAPPED
MAY ALSO FEATURE LINE-SIDE COMMON-MODECHOKE
TRANS_DATAPR
TD+
TCT
TD-
TX+
TCMT
TX-
RD+
RCT
RD-
RX+
RCMT
RX-
RJ45 PIN 4
RJ45 PIN 5
RJ45 PIN 7
RJ45 PIN 8
1000PF CERAMIC 2KV
100NF 16V
100NF 16V
100R
100R
POWER_3V3
POWER_3V3
M-LVDS HALF-DUPLEX TRANSCEIVER
M-LVDS HALF-DUPLEX TRANSCEIVER
CLK_A TRANSMIT ENABLE (DEFAULT = ACTIVE)
CLK_A TRANSMIT
CLK_A RECEIVE
CLK_B TRANSMIT ENABLE (DEFAULT = INACTIVE)
CLK_B TRANSMIT
CLK_B RECEIVE
SIGNALS TO HRMAI LOGIC

Fig 42

Octet	Content
0-7	Preamble and start frame delimiter (55_{16} 55_{16} 55_{16} 55_{16} 55_{16} 55_{16} 55_{16} D_{16})
8-13	MAC destination address (default = 80_{16}-00_{16}-00_{16}-00_{16}-00_{16}-00_{16})
14-19	MAC source address (default = 00_{16}-00_{16}-00_{16}-00_{16}-00_{16}-00_{16})
20-21	Length/Type field (05_{16}-$8E_{16}$)
22-24	LLC header (AA_{16}-AA_{16}-03_{16})
25-29	SNAP header (value to be determined)
30-35	Frame format identification header
36-1443	Payload
1444-1447	32-bit frame CRC (ISO/IEC 8802.3)

Fig 43

	Bits 0:3	Bits 4:7
Octet 30	Protocol minor version	Protocol major version
Octet 31	Frame Type	Flags
Octet 32	Audio Format	
Octet 33	(reserved)	
Octet 34	(reserved)	
Octet 35	CRC-8 checksum	

Fig 44A

Value	Frame type
0_{16}	Frame contains bitstream-mode audio
1_{16}	Frame contains AES3-compatible mode audio
(other)	(reserved – frame shall be disregarded by receiver)

Fig 44B

Bit	Flag indication
0	0: (no flag)
	1: first sample in frame is associated with an Audio sample synchronisation marker (see section 9.3)
3:1	(reserved: transmitted as zero, disregarded by receiver)

Fig 44C

Bit	Flag indication
0	0: (no flag)
	1: first sample in frame is associated with an Audio sample synchronisation marker (see section 9.3)
3:1	(reserved: transmitted as zero, disregarded by receiver)

Fig 44D

Value	Flag indication
61_{16}	Frame contains bit-stream audio: 1-bit samples, $64f_s$ sample rate
71_{16}	Frame contains bit-stream audio: 1-bit samples, $128f_s$ sample rate
(other)	(reserved – frame shall be disregarded by receiver)

Fig 44E

Bits	Flag indication
3:0	Sample word length: (unsigned 4-bit integer, n) sample word length = 4n
5:4	Sample frequency multiplier: 00_2: 1x base frequency 01_2: 2x base frequency 10_2: 4x base frequency 11_2: 8x base frequency
6	Base sample frequency: 0: 44,1 kHz 1: 48 kHz
7	Variable sample frequency indicator: 0: Maximum sample frequency deviation = 100 ppm 1: Maximum sample frequency deviation = 12,5 %

Fig 44F

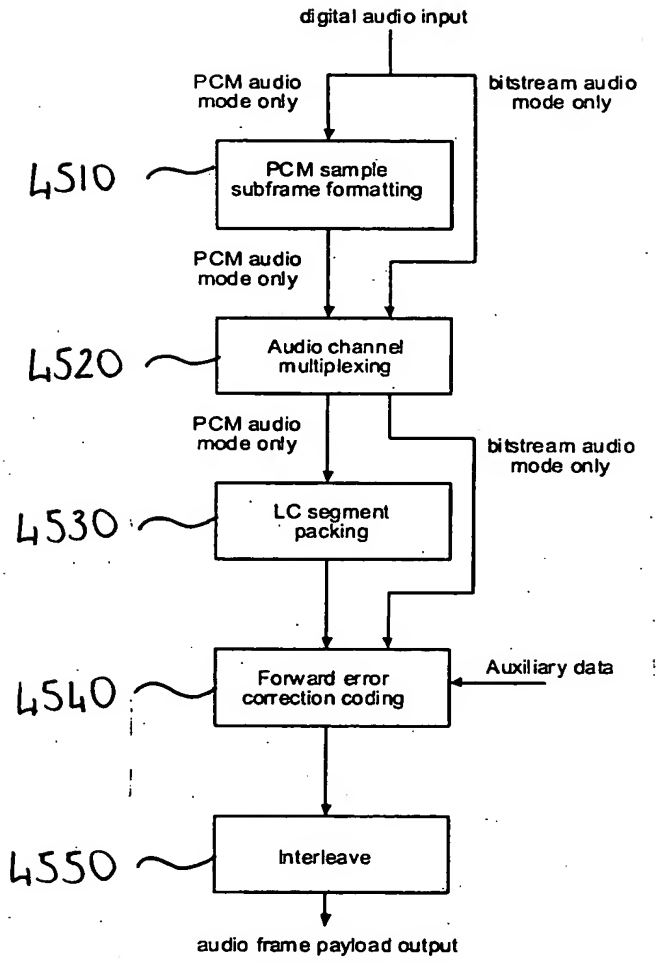

digital audio input
PCM audio mode only
bitstream audio mode only
4510
PCM sample subframe formatting
PCM audio mode only
4520
Audio channel multiplexing
PCM audio mode only
bitstream audio mode only
4530
LC segment packing
Auxiliary data
4540
Forward error correction coding
4550
Interleave
audio frame payload output

Fig 45

B

0000000**1100**00000

Fig 46A

B

0000000**1000**00000

Fig 46B

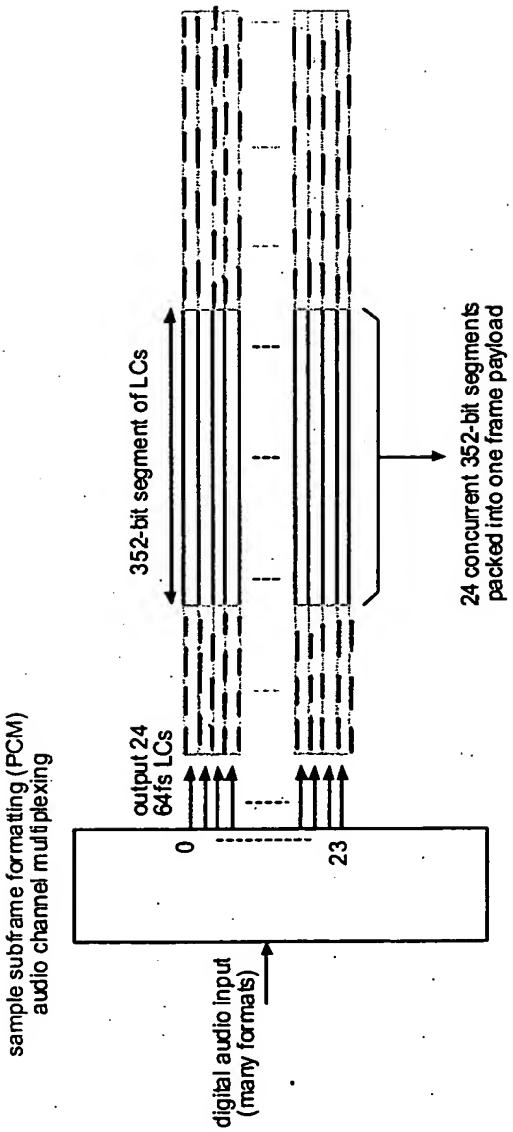

sample subframe formatting (PCM)
audio channel multiplexing
digital audio input
(many formats)
output 24
64fs LCs
0
23
352-bit segment of LCs
24 concurrent 352-bit segments
packed into one frame payload

Fig 47

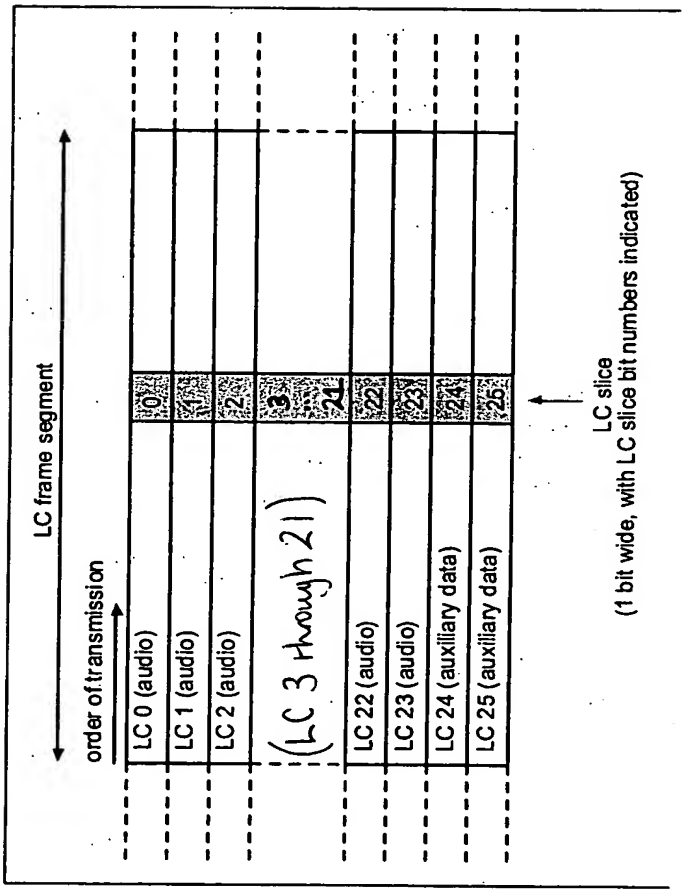

LC frame segment
order of transmission
LC 0 (audio)
LC 1 (audio)
LC 2 (audio)
(LC 3 through 21)
LC 22 (audio)
LC 23 (audio)
LC 24 (auxiliary data)
LC 25 (auxiliary data)
0
1
2
3
21
22
23
24
25
LC slice
(1 bit wide, with LC slice bit numbers indicated)

Fig 48

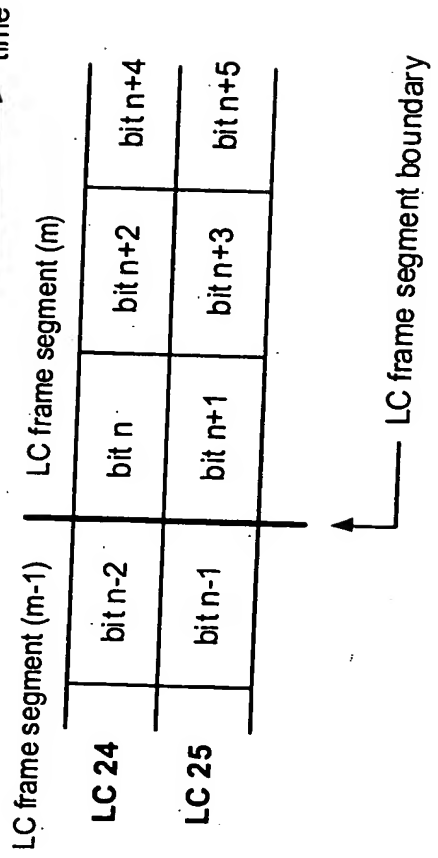

time
LC frame segment (m)
LC frame segment (m-1)
LC 24
LC 25
bit n-2
bit n
bit n+2
bit n+4
bit n-1
bit n+1
bit n+3
bit n+5
LC frame segment boundary

Fig 49

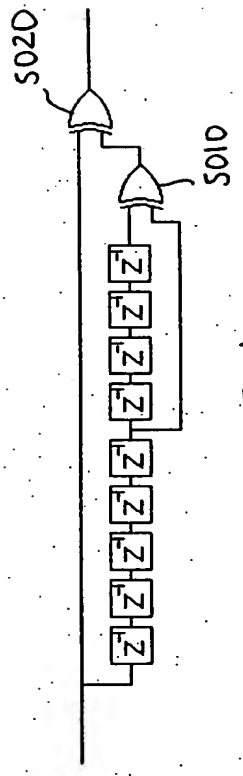


Fig 50A

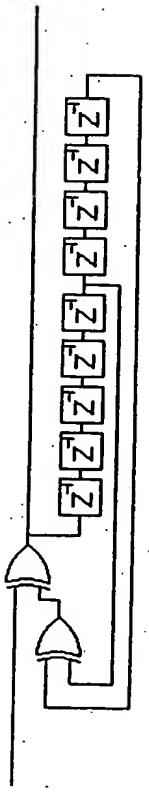


Fig. 50B

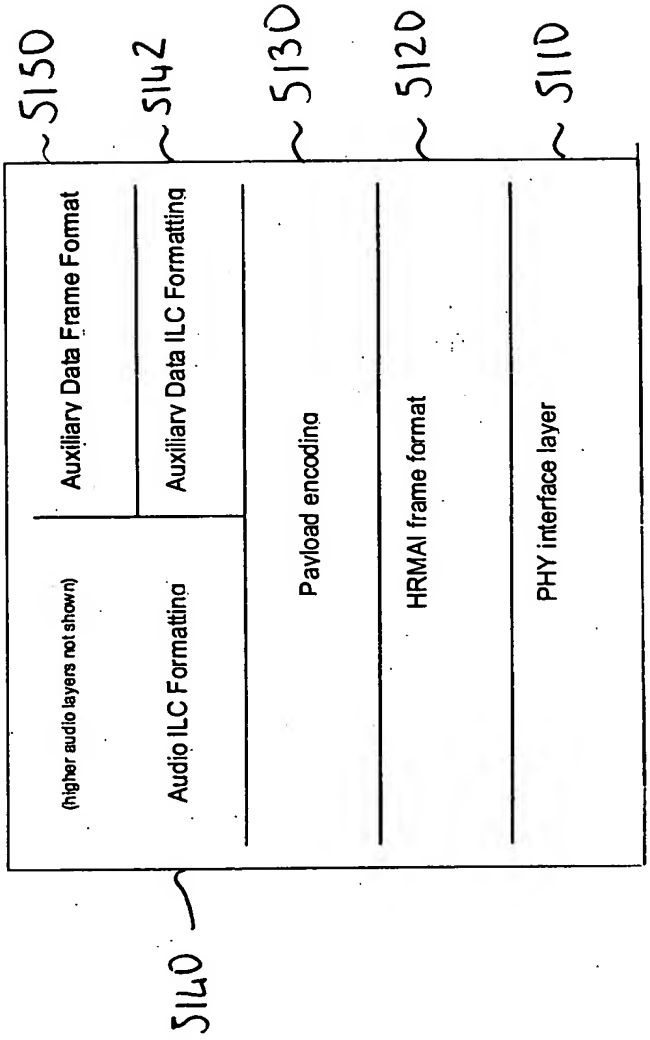

5150
5142
5130
5120
5110
Auxiliary Data Frame Format
Auxiliary Data ILC Formatting
Payload encoding
HRMAI frame format
PHY interface layer
(higher audio layers not shown)
Audio ILC Formatting
5140

Fig 51

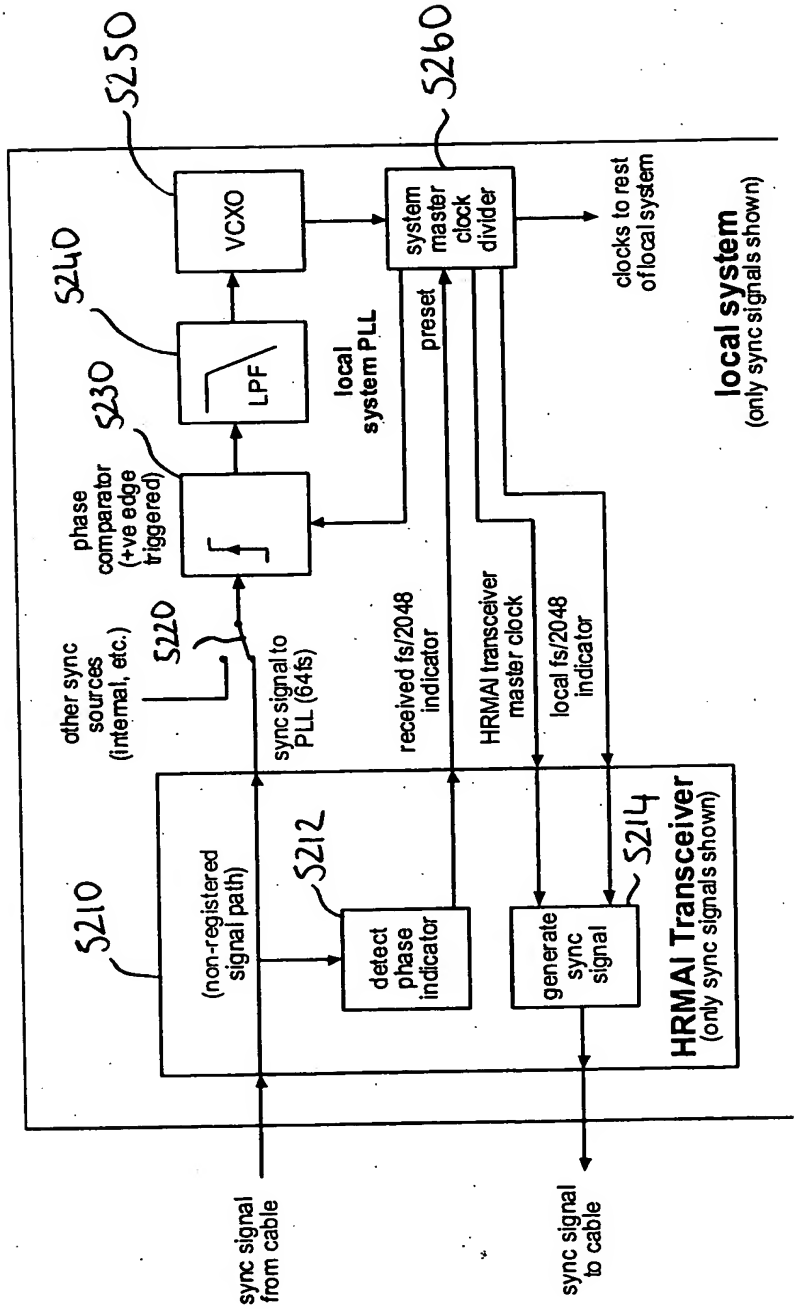

5250
5260
5240
5230
5220
5210
5212
5214
VCXO
LPF
phase comparator (+ve edge triggered)
local system PLL
preset
system master clock divider
clocks to rest of local system
local system
(only sync signals shown)
other sync sources (internal, etc.)
sync signal to PLL (64fs)
received fs/2048 indicator
HRMAI transceiver master clock
local fs/2048 indicator
(non-registered signal path)
detect phase indicator
generate sync signal
HRMAI Transceiver
(only sync signals shown)
sync signal from cable
sync signal to cable

Fig 52

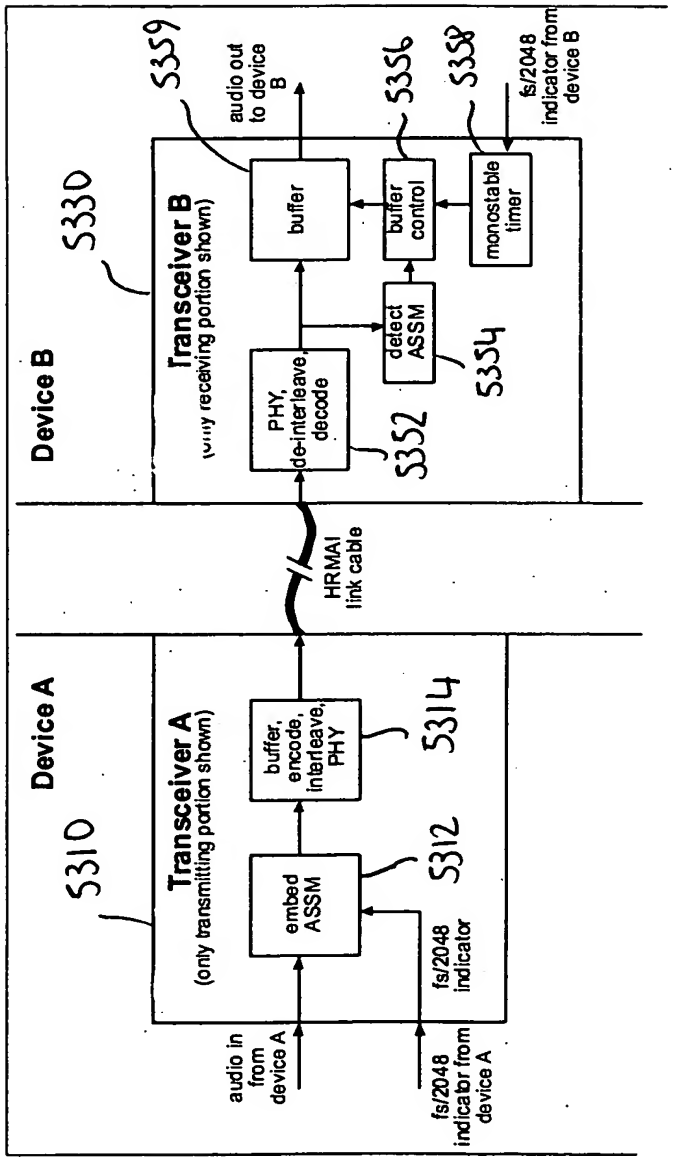

Device A
5310
Transceiver A
(only transmitting portion shown)
embed ASSM
5312
buffer, encode, interleave, PHY
5314
audio in from device A
fs/2048 indicator
fs/2048 indicator from device A
HRMAI link cable
Device B
5330
Transceiver B
(only receiving portion shown)
PHY, de-interleave, decode
5352
detect ASSM
5354
buffer
5359
buffer control
5356
monostable timer
5358
audio out to device B
fs/2048 indicator from device B

Fig 53